DESIGN AND DELIBERATION OF A TEN-TRANSISTOR SRAM CELL EMPLOYING HALF-VDD ROW-WISE DYNAMIC PRE-CHARGE FOR DIMINISHED SWITCHING POWER AND ULTRA-LOW READ BIT-LINE LEAKAGE

K. DEVAKI DEVI[1], M. ANUSHA[2],S. RUCHITHA[3], K. MOUNIKA[4], G. GOWTHAMI[5]
[1]Associative Professor, Dept. of ECE, V.K.R., V.N.B. & A.G.K. COLLEGE OF ENGINEERING, GUDIVADA.
[2345]UG Students, Dept. of ECE, V.K.R., V.N.B. & A.G.K. COLLEGE OF ENGINEERING, GUDIVADA

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ABSTRACT
This paper proposes a novel 10-transistor (10T) static random-access memory (SRAM) cell incorporating a single-ended, decoupled read bit line (RBL) supported by a dedicated 4-transistor read port to achieve low-power operation and significant leakage reduction. The RBL is precharged to half of the supply voltage (VDD/2) and subsequently allowed to either charge or discharge depending on the stored data value. During read operation, an inverter controlled by the complementary storage node (QB) connects the RBL to dynamically controlled virtual power rails through a transmission gate. For a stored logic '1', the RBL charges toward VDD, whereas for a stored logic '0', it discharges toward ground. In both hold and write modes, the virtual rails are maintained at the same potential as the RBL precharge level and are connected to the actual supply rails only during read access. This dynamic control of virtual rails effectively suppresses RBL leakage current. Implemented in a commercial 65 nm CMOS technology, the proposed 10T cell occupies 2.47 times the area of a conventional 6T SRAM cell with β = 2. It achieves a 2.3× improvement in read static noise margin (RSNM) and reduces read power dissipation by 50% compared to the 6T design. Furthermore, RBL leakage current is reduced by more than three orders of magnitude, and the ION/IOFF ratio is significantly enhanced relative to conventional bit-line leakage. Despite the additional transistors, the overall leakage characteristics remain comparable to the 6T cell while delivering competitive performance and improved robustness.

Keywords:T10T SRAM, Single-Ended Read Bit Line (RBL), Virtual Power Rails, Leakage Reduction, Low Power Design, Charge Recycling, Read Static Noise Margin (RSNM), 65 nm CMOS Technology

I INTRODUCTION
Static Random-Access Memory (SRAM) is a fundamental building block in modern System-on-Chip (SoC) architectures, contributing significantly to total chip area and energy consumption [1]. In advanced processors and embedded platforms, cache memories dominate the silicon footprint, compelling designers to maximize cell density and minimize peripheral overhead [2]. To improve area efficiency, multiple cells are connected along a single column so that sense amplifiers and decoders can be shared effectively [3]. However, as the number of cells per bit-line increases, cumulative leakage currents and reduced I_{ON}/I_{OFF}ratios limit reliable operation in conventional designs [4]. These effects are particularly pronounced in deeply scaled CMOS technologies, where leakage mechanisms intensify and device variability increases [5].
The traditional 6-transistor (6T) SRAM cell has been widely adopted due to its compact structure and differential sensing capability [6]. Nevertheless, the 6T topology suffers from read disturb issues because the

same access transistors are used for both read and write operations [7]. During a read cycle, the internal storage nodes are directly connected to precharged bit-lines, which can disturb the stored data, especially under low supply voltages [8]. As technology scales and supply voltages are reduced to control dynamic power, the static noise margin (SNM) degrades substantially [9]. Consequently, ensuring robust read stability in long-column architectures becomes increasingly challenging [10].

To overcome these limitations, alternative SRAM topologies such as 8T, 9T, and 10T cells have been introduced [11]. These architectures typically decouple the read and write paths by incorporating dedicated read ports, thereby isolating the storage nodes from bit-line disturbances during read operations [12]. Such separation significantly enhances read static noise margin (RSNM) and improves reliability in low-voltage operation [13]. However, the additional transistors increase cell area and may introduce leakage overhead if not carefully optimized [14]. Therefore, a careful balance between robustness, area efficiency, and energy consumption is required [15].

Assist techniques have also been widely explored to improve SRAM stability [16]. Word-line underdrive reduces access transistor strength to mitigate half-selected cell disturbances [17]. Bit-line precharge modulation and negative bit-line techniques enhance read stability but may compromise write margin at lower supply voltages [18]. Supply boosting and ground biasing approaches further strengthen cell feedback during critical operations, yet they introduce additional circuit complexity and energy overhead [19]. Although assist schemes improve yield, they require precise timing control and are sensitive to process and temperature variations [20].

The growing demand for ultra-low-power electronics, including IoT nodes, wearable devices, and battery-powered sensors, has intensified research into near-threshold and sub-threshold SRAM operation [21]. Operating at reduced supply voltages significantly lowers dynamic energy consumption, which scales quadratically with voltage [22]. However, near-threshold operation reduces stored node charge, making cells more susceptible to noise, leakage, and transient disturbances [23]. Variability effects, including random dopant fluctuations and line-edge roughness, further degrade stability margins in nanometer technologies [24]. As a result, conventional SRAM cells become increasingly vulnerable under aggressive voltage scaling [25].

In addition to electrical challenges, radiation-induced effects pose serious reliability concerns in scaled CMOS circuits [26]. High-energy particles can deposit charge at sensitive storage nodes, leading to Single-Event Upsets (SEUs) or transient faults [27]. As node capacitance decreases with technology scaling, the critical charge required to flip a bit also decreases, increasing the soft error rate [28]. These issues are particularly critical in aerospace, medical, and safety-sensitive applications where data integrity is paramount [29]. Therefore, enhancing SRAM resilience against both electrical disturbances and radiation effects has become an essential research focus [30].

Radiation-Hardened-By-Design (RHBD) techniques provide a practical solution by embedding robustness at the circuit and layout levels using standard CMOS processes. By incorporating decoupled read paths, reinforced feedback structures, transistor stacking, and node capacitance enhancement, modern SRAM architectures can achieve improved stability without sacrificing low-power operation. Integrating these strategies enables scalable, energy-efficient, and reliable memory designs suitable for next-generation SoC platforms operating in both terrestrial and radiation-prone environments.

II LITERATURE SURVEY

Static Random-Access Memory (SRAM) is a critical component in modern System-on-Chip (SoC) architectures, accounting for a substantial portion of total chip area and energy consumption [1]. With aggressive CMOS scaling, reducing supply voltage has become an effective approach for minimizing dynamic power dissipation [2]. Subthreshold SRAM designs demonstrated the feasibility of ultra-low-voltage operation, achieving stable functionality at significantly reduced supply levels [3]. However, technology scaling introduces severe variability and leakage challenges that degrade stability margins in conventional 6T SRAM cells [4]. To address manufacturability and reliability concerns, stabilizing circuits were incorporated into embedded SRAM arrays, improving read and write robustness [5]. Peripheral assist techniques have further enabled 6T SRAM operation down to deep submicron voltage levels while maintaining acceptable performance [6].

Despite these improvements, conventional 6T cells suffer from read disturb issues due to shared read and write paths. Alternative cell topologies such as 8T SRAM were introduced to decouple read and write operations, thereby improving read stability [7]. Assist techniques supporting wide voltage operation have been extensively

explored to enhance robustness under process and temperature variations [8]. Advanced SOI-based SRAM designs achieved reliable low-voltage functionality by strengthening write-ability and read-ability margins [9]. Dynamic cell biasing was proposed to enhance fluctuation tolerance in sub-600 mV SRAM arrays, highlighting the importance of adaptive control schemes [10].

Selective precharge techniques were developed to improve read stability while limiting energy overhead [11]. Differential 8T SRAM cells improved noise margins and supported bit-interleaving for enhanced reliability [12]. Half-select disturbance was mitigated in 9T SRAM designs, enabling reliable supply voltage scaling without compromising array density [13]. Single-ended disturb-free 9T SRAM architectures further enhanced subthreshold operation through adaptive read timing and negative bit-line techniques [14]. Minimum supply voltage reduction was achieved in 8T SRAM through VDD-min-enhancing assist circuits, demonstrating improved stability at low voltages [15]. Variability-tolerant SRAM topologies were also proposed to sustain performance across process corners in scaled technologies [16].

Redundancy-based techniques were introduced to improve sensing reliability and tolerance to variation in subthreshold SRAM arrays [17]. Schmitt-trigger-based SRAM designs enhanced noise immunity and process variation tolerance at ultra-low voltages [18]. Single-ended 10T SRAM cells were proposed for low-power applications, offering improved leakage control and read stability compared to conventional 6T designs [19]. Stability enhancements for 32 nm and beyond highlighted the need for cell-level and peripheral-level co-optimization [20]. Process variation analysis in embedded memories emphasized architecture-aware solutions to improve yield and robustness [21]. Fundamental device scaling studies revealed physical limitations that directly impact SRAM performance and reliability [22].

Beyond electrical variability, radiation-induced soft errors have emerged as a major reliability concern in scaled technologies. Soft error characterization studies showed increasing susceptibility of CMOS latches and memory cells to particle strikes [23]. Comprehensive analyses of radiation sources and mechanisms further clarified their impact on advanced semiconductor devices [24]. Experimental evaluations of radiation-induced soft error rates in bulk CMOS confirmed the growing vulnerability of scaled memory arrays [25]. Foundational work on radiation effects established theoretical models for charge collection and upset phenomena in electronic systems [26]. Radiation effects in advanced microelectronics were shown to cause transient and permanent faults, particularly in dense SRAM structures [27].

As technology nodes continue to shrink, the critical charge required to flip stored data decreases, increasing the soft error rate in memory circuits [28]. Circuit-level mitigation techniques have been proposed to reduce soft error sensitivity while preserving performance [29]. Finally, reliability assessments under technology scaling have underscored the importance of combining low-power design with radiation-hardened strategies to ensure dependable SRAM operation in both terrestrial and harsh environments [30].

III METHODOLOGY

The methodology adopted for the proposed 10T adiabatic SRAM design is structured to achieve low power consumption, improved read stability, and controlled switching losses while maintaining architectural flexibility.

Initially, the conventional 6T SRAM cell was analysed to identify major limitations such as read disturb issues, high dynamic power dissipation due to full voltage swing, and leakage currents in scaled technologies. Based on this analysis, a 10-transistor (10T) topology was selected to decouple the read path from the storage nodes. The storage core was designed using two cross-coupled inverters to ensure bistable data retention. Additional transistors were incorporated to form a dedicated read port, thereby isolating internal nodes from direct bit-line interaction during read operations. This structural modification enhances read stability and prevents destructive read effects.

To implement adiabatic operation, trapezoidal power-clock waveforms were introduced instead of conventional DC supply signals. The trapezoidal waveform enables gradual charging and discharging of capacitive nodes, thereby reducing instantaneous current flow and minimizing short-circuit currents. The rise and fall slopes of the waveform were carefully controlled to ensure near-adiabatic energy transfer. By slowing down voltage transitions, the energy dissipated across channel resistance is significantly reduced, following adiabatic switching principles.A midpoint precharge strategy was also incorporated for the read bit-line. Instead of precharging the bit-line to full supply voltage, it was precharged to approximately half of the supply voltage. During read operations, only a small voltage deviation around this midpoint was generated depending on the

stored data. This reduced voltage swing approach directly lowers dynamic power consumption, as energy dissipation is proportional to the square of voltage swing. Furthermore, dynamically controlled virtual power rails were introduced to suppress leakage currents during standby and write modes. These virtual rails ensure minimal voltage difference across inactive transistors, thereby reducing subthreshold leakage.

Device sizing was optimised to balance noise margin, leakage control, and switching speed. Transistor width-to-length ratios were selected to maintain sufficient drive strength for read operations while preventing excessive static current. Particular attention was given to the pull-down and read-access transistors to maintain reliable sensing under low-voltage conditions.

The proposed design was evaluated using circuit-level simulations under varying supply voltages and operating conditions. Key performance metrics such as dynamic power consumption, static leakage power, read static noise margin (RSNM), and propagation delay were measured and compared with conventional SRAM architectures. Energy dissipation per read/write cycle was calculated to assess efficiency improvements. Area overhead due to additional transistors and adiabatic control circuitry was also estimated.

IV PROPOSED METHOD

The proposed system introduces a robust and low-power 10-transistor (10T) SRAM bit cell architecture designed to overcome the read instability and leakage limitations of conventional 6T cells, particularly under low-voltage and near-threshold operation. The topology enhances the read static noise margin (RSNM), reduces data-dependent read bit-line (RBL) leakage, and improves the effective I_{ON}/I_{OFF}ratio, enabling reliable operation in long bit-line arrays.

Topology of the Proposed Bit Cell

The proposed bit cell retains the conventional cross-coupled inverter pair used for data storage but integrates a dedicated 4T read port to decouple the internal storage nodes from the read path. The storage core consists of two cross-coupled inverters formed by pull-up and pull-down transistors, ensuring bistable data retention. To enable isolated read functionality, four additional NMOS transistors are introduced in the read path.

The read port includes an inverter (P1–N1) driven by the complementary storage node (QB), followed by a transmission gate (P2–N2). The inverter output connects to the single-ended read bit-line (RBL) through the transmission gate during read operations. This configuration prevents direct interaction between internal storage nodes and the bit-line, eliminating read disturb effects common in conventional 6T SRAM.

A key feature of the topology is the use of dynamically controlled virtual power rails, denoted as VVDD and VVSS. These rails power the read port and are only connected to the true supply rails during read operations. During standby and write modes, VVDD and VVSS are maintained at the same voltage as the precharged RBL level. This approach effectively suppresses read port leakage currents and minimizes unnecessary power dissipation.

Bit Cell Working Mechanism

In deeply scaled technologies, the I_{ON}/I_{OFF}ratio degrades significantly, especially at low supply voltages. As more cells are connected to a single bit-line, cumulative leakage currents increase and approach the magnitude of the read current. This makes it difficult for the sense amplifier to accurately detect the RBL voltage level. Furthermore, conventional designs suffer from data-dependent leakage, where the stored data influences bit-line leakage, causing large variations in off-state current.

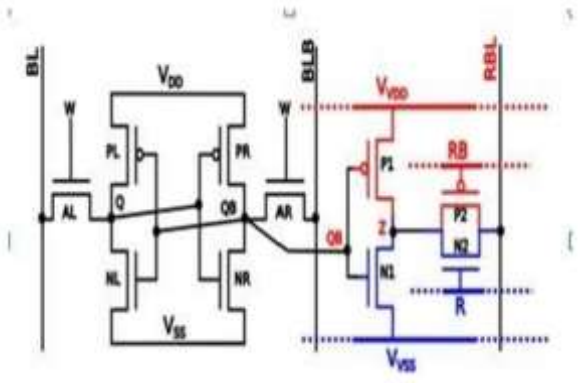

Fig.1 Proposed10TSRAMcellwithrow-wisereadportdynamicpowerlines

The proposed 10T cell addresses these issues by implementing a data-independent read mechanism. The RBL is precharged to $V_{DD}/2$, rather than to the full supply voltage. During a read operation, the read port either slightly charges or slightly discharges the RBL depending on the stored data. If the stored bit corresponds to logic '1', the RBL rises slightly above $V_{DD}/2$; if it corresponds to logic '0', the RBL falls slightly below $V_{DD}/2$. This symmetric voltage swing around the midpoint significantly reduces the required voltage excursion compared to full-swing designs.

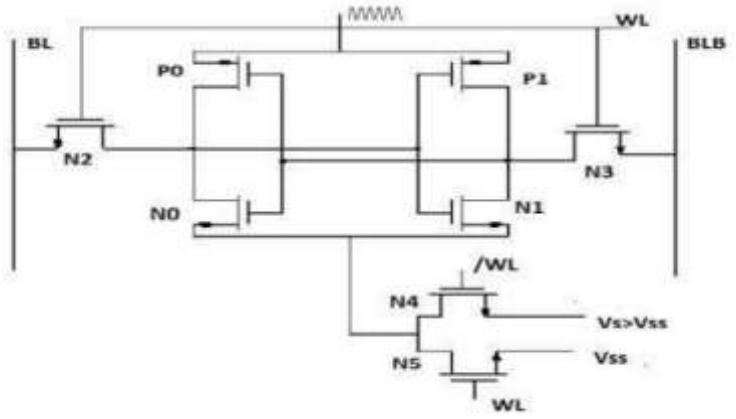

Fig.2 BasicAdiabaticSRAMcell

Unlike previous INV+TG-based 10T cells that eliminated precharge and forced full swing transitions from VDD to VSS, the proposed method generates only a small differential variation from the midpoint. This reduces dynamic power consumption and enhances sensing reliability. Importantly, if consecutive read bits are identical, the RBL experiences minimal change, further lowering switching activity and energy dissipation.

Dynamic control of the virtual rails ensures that leakage paths are suppressed when the cell is not actively reading. Since VVDD and VVSS match the precharged RBL level during standby, there is minimal potential difference across read transistors, thereby reducing subthreshold and gate leakage currents.

Power Dissipation Reduction Technique

Power dissipation in SRAM circuits consists of static and dynamic components. Dynamic power dominates due to repeated charging and discharging of bit-line capacitances. In conventional CMOS, each full voltage swing from 0 to V_{DD}dissipates energy proportional to $\frac{1}{2}C_L V_{DD}^2$. Reducing voltage swing is therefore an effective strategy for lowering energy consumption.

The proposed system incorporates an energy-efficient charging strategy inspired by adiabatic principles. By limiting the RBL swing to a small deviation around $V_{DD}/2$, the effective charging energy is significantly reduced. Since the voltage transition is partial rather than full swing, both charging and discharging losses decrease.

Additionally, dynamic rail control prevents unnecessary static leakage during standby. By eliminating large voltage differences across inactive transistors, subthreshold leakage and gate tunneling currents are minimized. The absence of full-swing transitions further reduces switching losses.

V SIMULATION RESULTS

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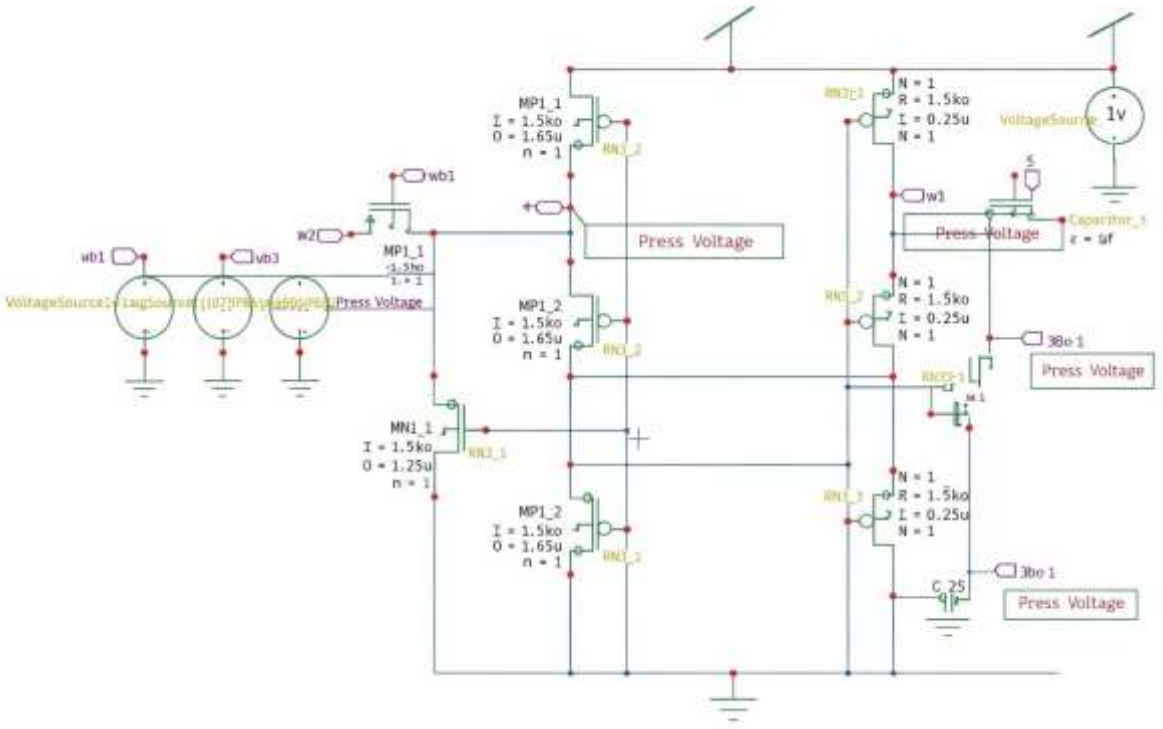

Fig.3 Proposed method of SRAM Cell

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Power Results

Total Power from time 0 to 1e-007
Average power consumed -> 1.374448e-004 watts
Max power 1.801058e-004 at time 4.1e-008
Min power 8.108652e-005 at time 4.05227e-008


Parsing                          0.01 seconds
Setup                            0.01 seconds
DC operating point               0.09 seconds
Transient Analysis               0.01 seconds
Overhead                         0.63 seconds
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Total                            0.75 seconds
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Fig.4 Calculationofproposedmethod

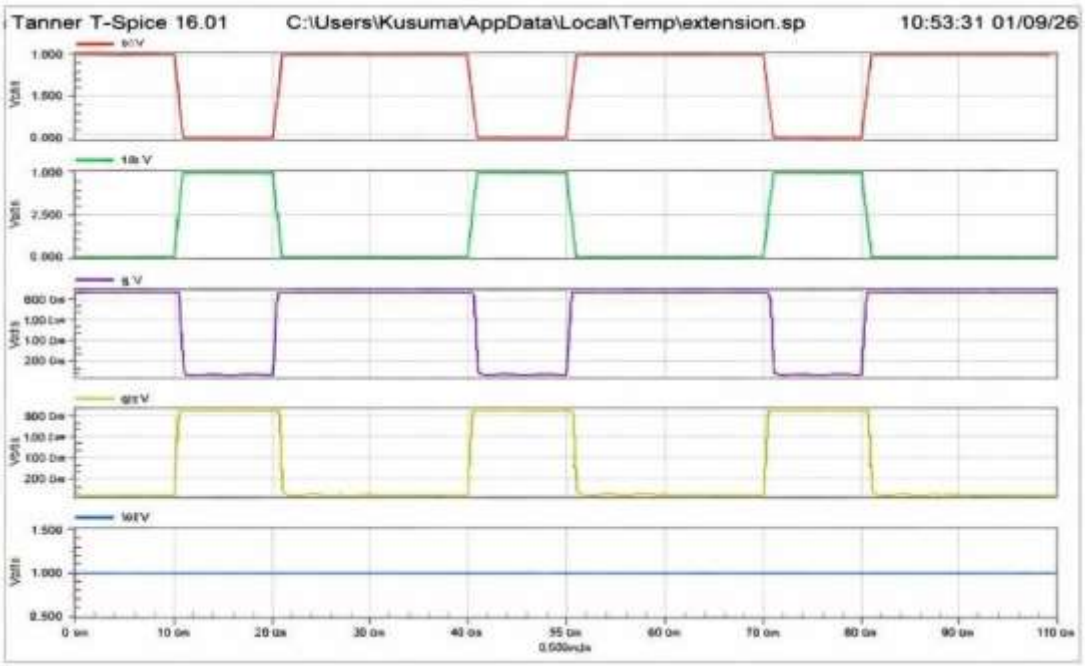

Fig.5 Waveformsofproposedmethod

VI CONCLUSION

The proposed 10T adiabatic SRAM architecture presents an energy-efficient memory solution tailored for low-power and mobile applications. By integrating adiabatic logic principles, the design minimizes energy dissipation during switching operations through controlled charging and discharging using trapezoidal power-clock waveforms. This technique significantly reduces short-circuit currents and dynamic power consumption compared to conventional SRAM structures. The gradual energy transfer mechanism makes the circuit particularly suitable for applications where delay constraints are not critical, thereby enabling efficient operation without excessive complexity.The results demonstrate that the core advantage of adiabatic logic—reduced power dissipation—is successfully achieved in the proposed SRAM design. However, certain trade-offs are observed. The noise margin is reduced by approximately 54%, and the structural area increases by nearly four times due to additional transistors and control circuitry. Despite these limitations, the architecture remains adaptable and can be optimized according to system-level requirements.

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