

DESIGN OF A VOLTAGE-RESILIENT KEEPER-BASED FULL ADDER USING CMOS TECHNOLOGY

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ABSTRACT

This paper presents the design of a voltage-resilient Static Adaptive Energy (SAE) keeper-based full adder implemented using CMOS technology to achieve high speed, low power consumption, and robust operation under scaled supply voltages. The proposed architecture employs a keeper-assisted XOR–XNOR cell to overcome the critical challenge of maintaining full-swing output voltage in low-voltage environments. By incorporating an optimized grounded keeper configuration derived from conventional 20-transistor structures, the design significantly reduces transistor count while enhancing performance metrics. The proposed 16-transistor full adder is simulated using TSPICE in 90-nm CMOS technology and evaluated across a wide supply voltage range from 0.6 V to 1.5 V. Performance comparison with existing keeper-based designs is carried out in terms of power dissipation, propagation delay, and power-delay product (PDP). Simulation results demonstrate that the proposed architecture achieves lower power consumption, reduced delay, and improved PDP across all operating voltages, confirming superior voltage resilience. The effectiveness of the design is further validated through implementation in a 4-bit ripple carry adder, making it suitable for low-power and high-speed VLSI applications including arithmetic logic units, multipliers, calculators, and graphical processing units.

Keywords: Full adder-Hybrid logic design-Keeper circuit-Logical effort-Voltage resilient -Ripple carry adder

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I INTRODUCTION

The advancement of Very Large Scale Integration (VLSI) technology has enabled the integration of millions of transistors onto a single silicon chip, thereby increasing computational capability while reducing device dimensions [1]. However, technology scaling has introduced significant design challenges, particularly in terms of power dissipation, signal integrity, and voltage reliability [2]. As CMOS devices enter deep-submicron regimes, supply voltage scaling becomes essential to limit dynamic power consumption, which is proportional to the square of the supply voltage [3]. Despite its advantages, voltage scaling leads to threshold voltage drop, reduced noise margins, and degraded voltage swing at internal circuit nodes [4]. These issues become increasingly critical in arithmetic circuits where logic stages are cascaded [5]. Furthermore, interconnect parasitics, routing congestion, and layout-dependent effects significantly influence circuit delay and robustness

in back-end implementation [6]. Therefore, logic circuits must be optimized at the transistor level not only for functional correctness but also for power efficiency, area minimization, and reliable physical realization [7]. These requirements have motivated extensive research into robust low-power arithmetic circuit design methodologies [8].

Among arithmetic components, the full adder serves as the fundamental building block in digital systems such as arithmetic logic units (ALUs), multipliers, digital signal processors, and microprocessors [9]. A full adder performs the addition of three binary inputs—A, B, and C_{in} —and produces two outputs, SUM and C_{out} [10]. Since multi-bit arithmetic structures such as ripple carry adders, carry look-ahead adders, and array multipliers are constructed using cascaded full adders, the efficiency of the overall system is directly determined by the performance of the individual adder cell [11]. Power consumption, propagation delay, and voltage stability of the SUM and C_{out} outputs strongly influence system throughput and reliability [12]. Numerous logic styles including conventional CMOS logic, pass transistor logic (PTL), transmission gate logic, and hybrid logic have been explored for full adder implementation [13]. While conventional CMOS provides full voltage swing and strong driving capability, it typically requires higher transistor count [14]. Pass transistor and hybrid logic styles reduce transistor count and power consumption but suffer from threshold voltage loss and degraded logic levels [15]. Consequently, achieving a balanced trade-off between power, delay, transistor count, and voltage reliability remains a primary objective in full adder design research [16].

One of the major challenges in low-voltage CMOS adders is voltage swing degradation at internal nodes, especially in designs employing NMOS or PMOS pass transistors [17]. NMOS devices pass strong logic '0' but weak logic '1', while PMOS devices pass strong logic '1' but weak logic '0' due to threshold voltage limitations [18]. When such degraded outputs are fed into subsequent stages, as in ripple carry structures, cumulative voltage loss leads to increased propagation delay and potential logic errors [19]. Reduced voltage swing also lowers noise margins and increases susceptibility to process variations and temperature fluctuations [20]. Moreover, leakage currents become prominent at reduced supply voltages, further affecting static power dissipation and reliability [21]. Conventional keeper circuits have been introduced to maintain logic levels and restore degraded voltages by weakly holding node states [22]. However, traditional keeper-based designs often increase transistor count and may introduce additional contention current, impacting power efficiency [23]. Therefore, a carefully optimized keeper mechanism is necessary to preserve full voltage swing without sacrificing speed or increasing area overhead [24].

To address these limitations, Static Adaptive Energy (SAE) keeper-based logic has emerged as a promising alternative for voltage-resilient arithmetic circuit design [25]. SAE logic operates in a fully static manner without requiring dynamic precharge phases, thereby eliminating charge sharing and clock-related complexity [26]. By incorporating optimized NMOS and PMOS keeper transistors, SAE circuits adaptively reinforce logic levels and restore voltage degradation at critical nodes [27]. This approach enhances noise immunity, improves reliability under voltage scaling, and reduces leakage power [28]. Additionally, reducing transistor count through intelligent restructuring of XOR–XNOR cells significantly lowers switching capacitance and dynamic power dissipation [29]. Optimization of transistor sizing based on logical effort principles further improves propagation delay and power-delay product (PDP) [30]. Consequently, SAE keeper-based full adders provide an effective solution for designing low-power and high-speed arithmetic units suitable for advanced VLSI systems.

Motivated by these challenges and research developments, this work proposes a voltage-resilient SAE keeper-based full adder with reduced transistor count and enhanced performance. The proposed architecture employs a grounded keeper configuration integrated within an optimized XOR–XNOR cell to ensure full-swing SUM and C_{out} outputs across a wide supply voltage range. Unlike conventional 20-transistor keeper-based designs, the proposed 16-transistor structure minimizes

hardware complexity while maintaining robust logic levels and improved propagation characteristics. The design is implemented using 90-nm CMOS technology and simulated using Tanner EDA tools to evaluate power dissipation, delay, and waveform integrity under supply voltage and temperature variations. Performance comparison with existing state-of-the-art designs confirms reduced power consumption, lower propagation delay, and superior power-delay product. Furthermore, the proposed full adder is validated in a 4-bit ripple carry adder configuration to demonstrate its practical applicability in scalable arithmetic systems. Thus, the presented voltage-resilient full adder architecture contributes toward the development of energy-efficient, reliable, and high-performance VLSI arithmetic units for modern computing applications.

II LITERATURE SURVEY

The design of low-power and high-performance CMOS circuits has been extensively investigated over the past three decades due to continuous technology scaling and increasing system complexity. Foundational texts on CMOS VLSI design established the principles of transistor sizing, interconnect optimization, and power-aware design methodologies [1], [2]. Early research highlighted that dynamic power consumption, proportional to switching capacitance and the square of the supply voltage, dominates digital circuits and can be reduced through voltage scaling and architectural optimization [3]. However, deep-submicron technologies introduced leakage power as a significant contributor to total energy consumption, particularly due to subthreshold leakage and gate oxide tunneling effects [4]. Techniques such as dual-threshold voltage assignment were proposed to balance performance and leakage reduction [5]. Furthermore, physical design challenges such as interconnect delay, parasitic capacitance, and layout density became critical factors influencing circuit reliability and timing closure [6]. Comprehensive circuit-level design methodologies were therefore developed to ensure that transistor-level optimizations translate effectively into manufacturable layouts [7]. Standard CMOS digital circuit analysis frameworks provided structured approaches to delay modeling, noise margin evaluation, and robustness assessment under scaled supply voltages [8]. These foundational studies laid the groundwork for improving arithmetic building blocks, particularly full adders, which significantly impact overall system performance.

Extensive research has focused on optimizing full adder cells because they serve as fundamental components in arithmetic logic units, multipliers, and signal processing architectures [9], [10]. Early comparative studies analyzed different logic styles to determine trade-offs between power, delay, and transistor count in submicron technologies [11]. Reviews of 0.18- μm and smaller technology nodes revealed that transistor sizing and logic topology strongly influence power-delay product (PDP) and output voltage swing [12]. Hybrid full adder designs combining CMOS logic with pass transistor techniques were introduced to reduce transistor count while maintaining acceptable performance [13]. Performance evaluations of low-power CMOS full adders demonstrated that careful optimization of pull-up and pull-down networks can reduce short-circuit currents and improve switching speed [14]. Energy-efficient arithmetic cells were further developed to address the increasing demand for battery-powered and portable devices [15]. Researchers proposed novel XOR–XNOR gate implementations to improve SUM generation while minimizing propagation delay [16]. Low-voltage CMOS full adders were specifically examined for operation near threshold voltage levels, highlighting the importance of robust logic restoration [17]. Comparative investigations between conventional CMOS and pass transistor logic emphasized that while pass transistor circuits offer reduced area and capacitance, they suffer from threshold voltage degradation and reduced output swing [18]. Advanced compressor architectures were also explored to enhance arithmetic performance in multipliers, where full adders form essential sub-blocks [19]. These studies collectively demonstrate that full adder optimization remains central to improving digital arithmetic systems.

A significant body of literature addresses voltage scaling and leakage control techniques aimed at maintaining circuit functionality under reduced supply voltages. Dynamic threshold voltage scaling

and adaptive body biasing methods were introduced to suppress leakage currents without significantly compromising performance [20]. Comprehensive analyses of nanometer CMOS leakage mechanisms emphasized the necessity of power-aware design strategies in scaled technologies [21]. Glitch reduction and switching activity minimization techniques were proposed to lower unnecessary dynamic power dissipation in combinational circuits [22]. Keeper-based logic emerged as a promising solution to address voltage degradation at dynamic or high-impedance nodes by weakly maintaining logic levels [23]. Early multi-threshold CMOS (MTCMOS) techniques demonstrated that careful threshold voltage assignment could enable reliable operation at supply voltages as low as 1 V while maintaining high speed [24]. Further studies investigated ultra-dynamic voltage scaling (UDVS), which leverages subthreshold operation to significantly reduce energy consumption in low-performance modes [25]. Research also identified leakage power as a limiting factor in future technology nodes, prompting exploration of adaptive and static power management schemes [26]. High-performance CMOS full adder designs incorporated improved transistor arrangements to balance drive strength and switching delay [27]. Meanwhile, power-conscious design methodologies emphasized reducing capacitive loading and optimizing logic depth to achieve energy-efficient arithmetic circuits [28]. Collectively, these investigations highlight that voltage resilience and leakage control are critical in ensuring reliable CMOS full adder operation under scaled supply voltages.

Another important direction in full adder research involves delay optimization through logical effort and transistor-level restructuring. The logical effort methodology provides a systematic framework to estimate propagation delay and optimize transistor sizing for balanced rise and fall times [29]. By applying logical effort principles, designers can minimize critical path delay and improve power-delay product in arithmetic circuits. Furthermore, power-aware design methodologies emphasize trade-offs between energy efficiency and performance in complex digital systems [30]. In this context, XOR–XNOR based adder architectures have received significant attention due to their ability to generate SUM outputs efficiently with reduced logic depth. However, pass transistor implementations often suffer from weak logic levels, which degrade noise margins and increase susceptibility to process variations. To mitigate these issues, researchers incorporated static keeper circuits that reinforce node voltages and restore degraded logic levels. Although keeper circuits improve voltage swing, they may introduce contention current if not carefully designed. Therefore, recent research efforts focus on adaptive keeper mechanisms that maintain logic integrity without significantly increasing power consumption or transistor count.

In summary, prior literature demonstrates that full adder performance is influenced by multiple interacting factors including transistor count, voltage swing integrity, leakage power, logical effort optimization, and supply voltage scaling. Conventional CMOS designs ensure full swing but incur higher area and power, while pass transistor and hybrid logic designs reduce transistor count at the expense of degraded voltage levels. Keeper-based techniques improve reliability but require careful optimization to avoid power overhead. Voltage scaling and leakage mitigation strategies further complicate design trade-offs, particularly in deep-submicron technologies. Consequently, there remains a need for a reduced-transistor, voltage-resilient full adder architecture that achieves full-swing outputs, low power dissipation, minimal propagation delay, and robust operation across wide supply voltage ranges. The proposed Static Adaptive Energy (SAE) keeper-based full adder builds upon the principles and findings reported in [1]–[30], aiming to integrate logical effort optimization, transistor count reduction, and adaptive keeper reinforcement into a unified architecture suitable for modern low-power, high-speed VLSI applications.

III METHODOLOGY

The methodology adopted in this work focuses on designing a voltage-resilient Static Adaptive Energy (SAE) keeper-based full adder using optimized CMOS transistor-level architecture. The design approach begins with analyzing limitations of conventional CMOS and hybrid full adder

structures, particularly issues related to degraded voltage swing, increased propagation delay, and higher transistor count. The objective is to reduce transistor count while preserving full-swing output and minimizing power dissipation. The proposed architecture is developed using a grounded keeper-based XOR–XNOR cell that ensures robust logic levels at internal nodes. The design process follows a bottom-up methodology starting from basic inverter validation, followed by XOR–XNOR cell design, and finally integration into a complete full adder structure. Logical effort principles are applied to optimize transistor sizing for balanced rise and fall times, thereby minimizing propagation delay along the critical path.

The first step in implementation involves designing and validating a CMOS inverter using 90-nm technology parameters in Tanner S-Edit and simulating it using T-Spice. This stage verifies correct switching operation, rise/fall time characteristics, and average power consumption. The inverter serves as a reference circuit for evaluating device strength and switching threshold levels. Following this, a keeper-assisted XOR–XNOR module is constructed. The XOR–XNOR cell is a critical block in full adder design because it generates intermediate signals required for SUM and CARRY computation. In conventional pass transistor implementations, XOR–XNOR circuits suffer from threshold voltage drop and weak logic levels. To overcome this limitation, a grounded keeper transistor is introduced to restore degraded voltage and maintain full swing. The keeper is carefully sized to avoid excessive contention current while ensuring stable logic retention at internal nodes.

In the next phase, the full adder core is developed using the optimized XOR–XNOR cell combined with NMOS and PMOS pull-up and pull-down networks. The SUM output is generated using cascaded XOR logic, while the CARRY output is implemented using an optimized majority function structure. The SAE mechanism ensures that internal dynamic nodes remain stable without requiring precharge phases. Unlike dynamic logic, the proposed circuit operates entirely in static mode, eliminating clock dependency and charge-sharing effects. Transistor count reduction is achieved by eliminating redundant transmission gates and merging logic functions wherever possible. The final design results in a 16-transistor structure compared to conventional 20-transistor implementations, thereby reducing switching capacitance and silicon area.

Simulation and performance evaluation constitute the next major step in the methodology. The circuit is simulated across a wide supply voltage range from 0.6 V to 1.5 V to evaluate voltage resilience. Transient analysis is performed to verify correct SUM and CARRY outputs for all eight input combinations of A, B, and CIN. Power analysis is carried out to measure average power consumption, maximum switching power, and leakage power components. Propagation delay is measured between input transitions and corresponding output responses to determine the critical path delay. Power–Delay Product (PDP) and Energy–Delay Product (EDP) are calculated to evaluate overall energy efficiency. Comparative simulations are conducted for conventional CMOS full adders, existing keeper-based adders, and the proposed SAE full adder under identical operating conditions to ensure fairness in evaluation.

Finally, the effectiveness of the proposed design is validated by implementing it in a 4-bit ripple carry adder (RCA) configuration. In the RCA structure, the CARRY output of one stage drives the CIN of the next stage, making voltage swing integrity critical. This configuration helps verify the robustness of the proposed adder under cascaded conditions. Waveform integrity, noise margin, and glitch reduction are carefully analyzed. Temperature and supply voltage variations are also examined to assess reliability under different operating conditions. The methodology demonstrates that careful transistor-level optimization combined with adaptive keeper logic significantly improves voltage stability, reduces power dissipation, and enhances speed performance, making the proposed full adder suitable for modern low-power VLSI applications.

IV PROPOSED SYSTEM DESCRIPTION

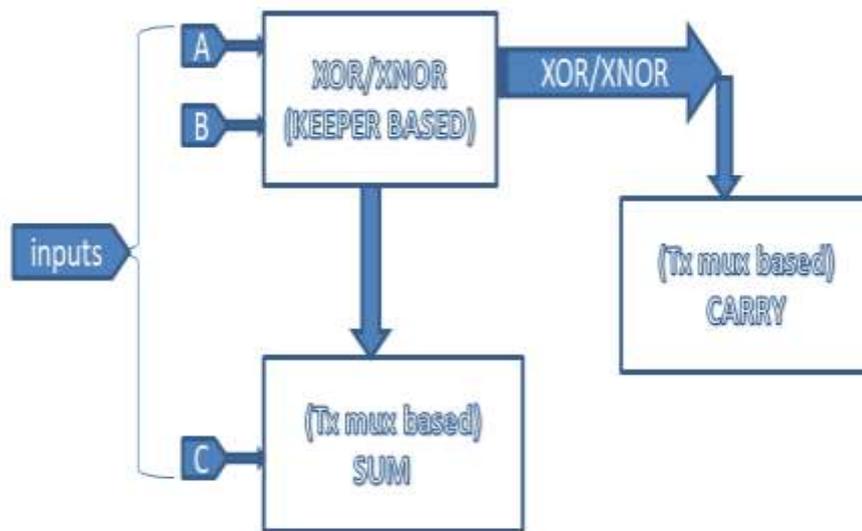
The proposed system is a 16-transistor Static Adaptive Energy (SAE) keeper-based full adder designed to achieve full voltage swing, low power consumption, and reduced propagation delay under scaled supply voltages. The architecture is built around an optimized XOR–XNOR cell integrated with a grounded keeper transistor to maintain voltage integrity at critical internal nodes. The design philosophy emphasizes minimizing transistor count without compromising logic robustness. By restructuring the logic equations of the full adder, redundant transistors are removed and logic sharing is introduced, resulting in a compact and energy-efficient configuration. The circuit operates entirely in static CMOS mode, eliminating the need for clock-driven precharge phases and ensuring continuous logic evaluation.

The XOR–XNOR module forms the core of the proposed full adder. This block generates intermediate signals ($A \oplus B$) and its complement, which are used to compute both SUM and CARRY outputs. In traditional pass transistor logic, threshold voltage loss leads to weak logic levels, especially when NMOS devices attempt to pass logic '1'. To address this issue, the proposed design incorporates a grounded keeper transistor connected to internal nodes. The keeper provides a weak feedback path that reinforces the correct logic level after switching transitions. The transistor sizing of the keeper is carefully optimized to prevent excessive short-circuit current during switching while ensuring reliable voltage restoration. As a result, the XOR–XNOR outputs exhibit full-swing behavior across a wide supply voltage range.

The SUM output is generated by combining the intermediate XOR result with the carry input (CIN) using a second XOR stage. The CARRY output is implemented using an optimized majority logic expression that reduces logic depth and transistor stacking. The proposed configuration ensures that both SUM and CARRY outputs maintain strong drive capability and minimal delay. Reduced transistor stacking lowers resistance along the critical path, which directly contributes to improved switching speed. Additionally, minimizing internal capacitance decreases dynamic power consumption. The SAE-based design ensures that internal nodes do not float or experience charge leakage, thereby improving noise immunity and reliability during cascaded operation.

One of the key advantages of the proposed system is its voltage resilience. The design is capable of operating reliably across supply voltages ranging from 0.6 V to 1.5 V. At lower supply voltages, conventional full adders often exhibit degraded voltage levels and increased delay due to threshold voltage effects. However, the grounded keeper mechanism in the proposed design adaptively maintains stable logic levels even under near-threshold conditions. This makes the circuit highly suitable for low-power portable devices where supply voltage scaling is essential for energy savings. Furthermore, reduced transistor count decreases silicon area, making the design attractive for high-density VLSI integration.

To demonstrate scalability, the proposed full adder is integrated into a 4-bit ripple carry adder structure. In this configuration, the carry propagation path becomes the dominant delay component. The proposed design ensures that each stage provides a full-swing CARRY output, preventing cumulative voltage degradation across stages. Simulation results confirm stable waveform transitions, reduced glitches, and improved energy efficiency compared to conventional and existing designs. The reduced Power–Delay Product (PDP) and Energy–Delay Product (EDP) highlight the superior energy–speed trade-off achieved by the proposed system. Overall, the voltage-resilient SAE keeper-based full adder provides an effective solution for designing low-power, high-speed arithmetic circuits in advanced CMOS technologies and can be extended to arithmetic logic units, multipliers, and digital signal processing architectures.



Proposed Block Diagram

The proposed full adder architecture is designed using a keeper-based transmission and pass transistor logic style with a reduced transistor count of 16, aimed at achieving low power consumption, compact area, and reliable operation at low supply voltages. The architecture efficiently generates both SUM and CARRY outputs while maintaining signal integrity through the use of adaptive keeper transistors. The overall architecture consists of three major functional blocks: the XOR/XNOR logic block, the SUM generation block, and the CARRY generation block. The XOR/XNOR block computes the intermediate signal $A \oplus B$, which serves as a common input for both SUM and CARRY logic. This shared computation eliminates redundant logic and significantly reduces the number of transistors compared to conventional designs. The SUM output is generated using a transmission-gate and pass-transistor network that combines the intermediate XOR output with the input carry (C_{in}). This logic structure ensures fast switching and reduced capacitive loading. A weak keeper transistor is connected to the dynamic SUM node to preserve logic levels and prevent voltage degradation caused by leakage or charge sharing. The CARRY output is realized using a compact majority logic configuration implemented with transmission-gate and pass transistors. The architecture ensures that the CARRY signal is correctly propagated based on the input combinations of A, B, and C_{in} . A keeper transistor is employed at the CARRY node to maintain stability and suppress glitches during input transitions.

In the proposed architecture, keeper transistors are strategically placed only at critical nodes instead of across the entire circuit. These keepers are weakly sized to minimize contention with the evaluation network while still providing adequate charge retention. This selective placement significantly reduces static and dynamic power dissipation. Compared to the existing 20-transistor keeper-based full adder, the proposed 16-transistor architecture offers lower area, reduced power consumption, and improved speed. The simplified structure also enhances robustness against process, voltage, and temperature variations. Overall, the architecture of the proposed full adder achieves an optimal balance between power efficiency, performance, and reliability, making it highly suitable for low-power arithmetic units and energy-efficient VLSI applications.

V SIMULATION RESULTS AND WAVEFORMS

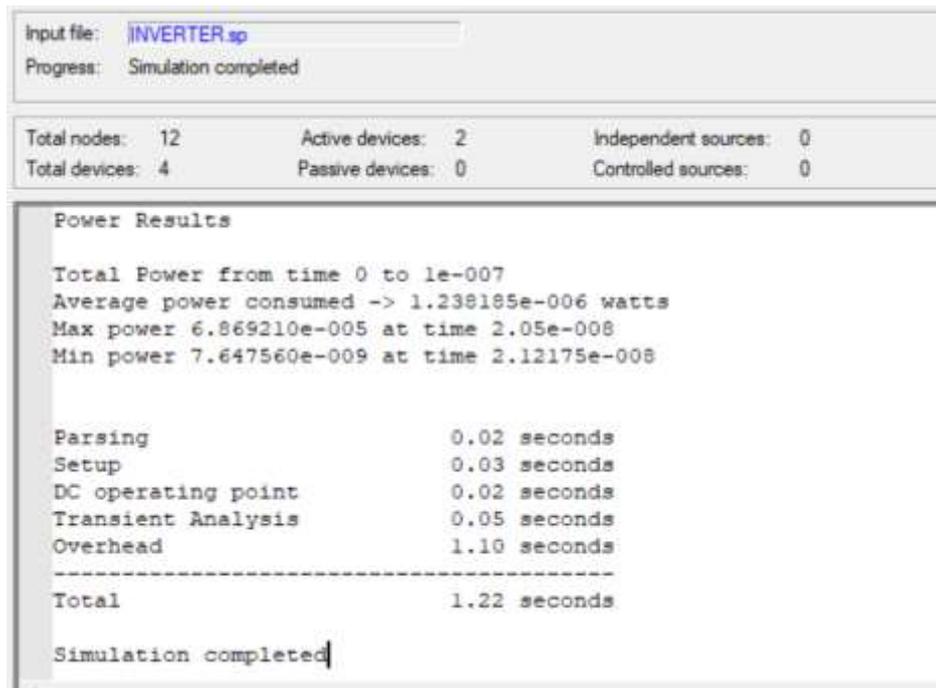


Fig 1: inverter simulation

The above results show the transient simulation of a CMOS inverter. The input is a square-wave signal, and the output waveform is its logical complement, confirming correct inverter operation. When the input goes HIGH, the NMOS turns ON and the PMOS turns OFF, pulling the output to LOW; when the input goes LOW, the PMOS turns ON and the NMOS turns OFF, pulling the output to HIGH. The waveforms clearly show this inversion with small rise and fall transition times due to device capacitances. From the power analysis, the inverter consumes a very low average power of 1.238 μW , indicating good low-power performance. The maximum power ($\approx 68.7 \mu\text{W}$) occurs during switching instants because both NMOS and PMOS conduct briefly, while the minimum power ($\approx 7.65 \text{ nW}$) corresponds to steady-state conditions.

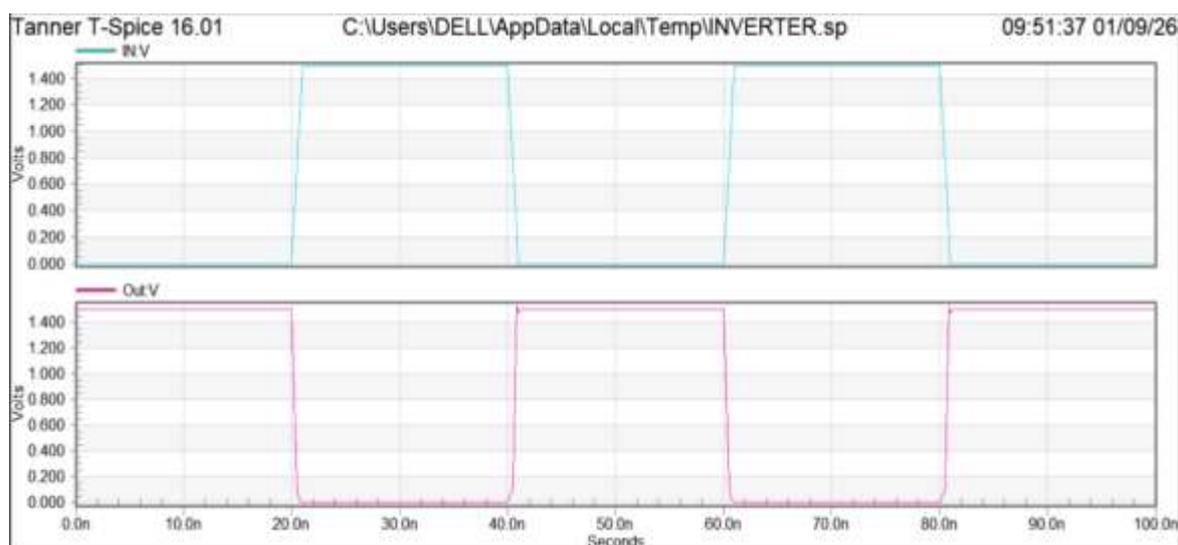


Fig 2: inverter output

Overall, the simulation verifies correct functionality, sharp switching behavior, and energy-efficient operation of the CMOS inverter.

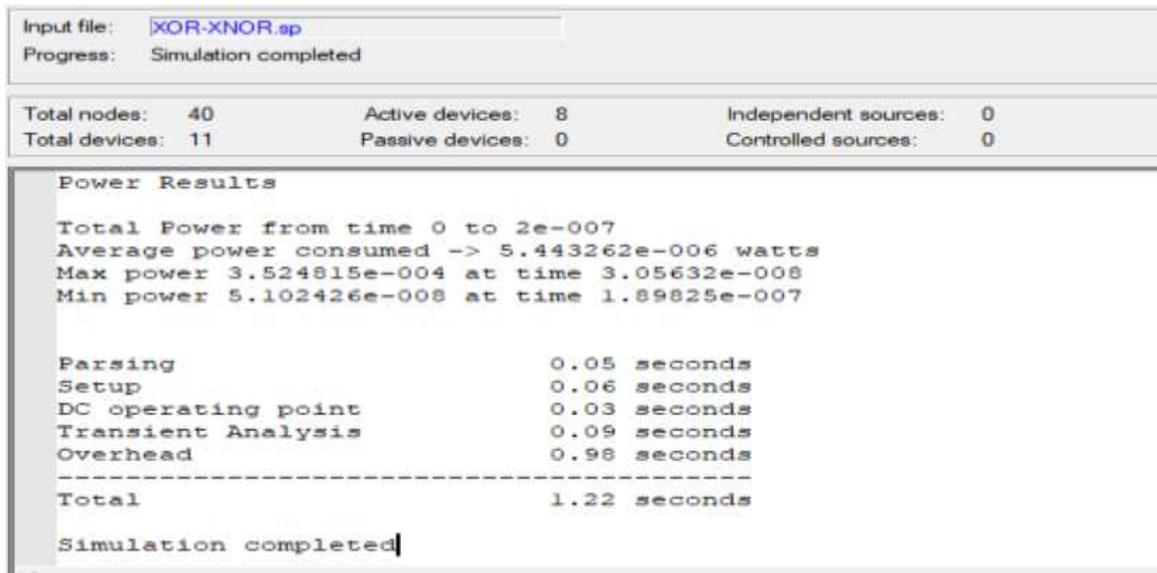


Fig 3: Xor/XnorSimulation

The above simulation shows the transient behavior of a CMOS-based XOR–XNOR circuit. Two input signals A and B are applied as square waves with different switching patterns. The waveforms confirm correct logic operation: the XOR output goes HIGH when the inputs are different ($A \neq B$), while the XNOR output goes HIGH when the inputs are the same ($A = B$). The complementary nature of XOR and XNOR is clearly visible in the timing diagrams.

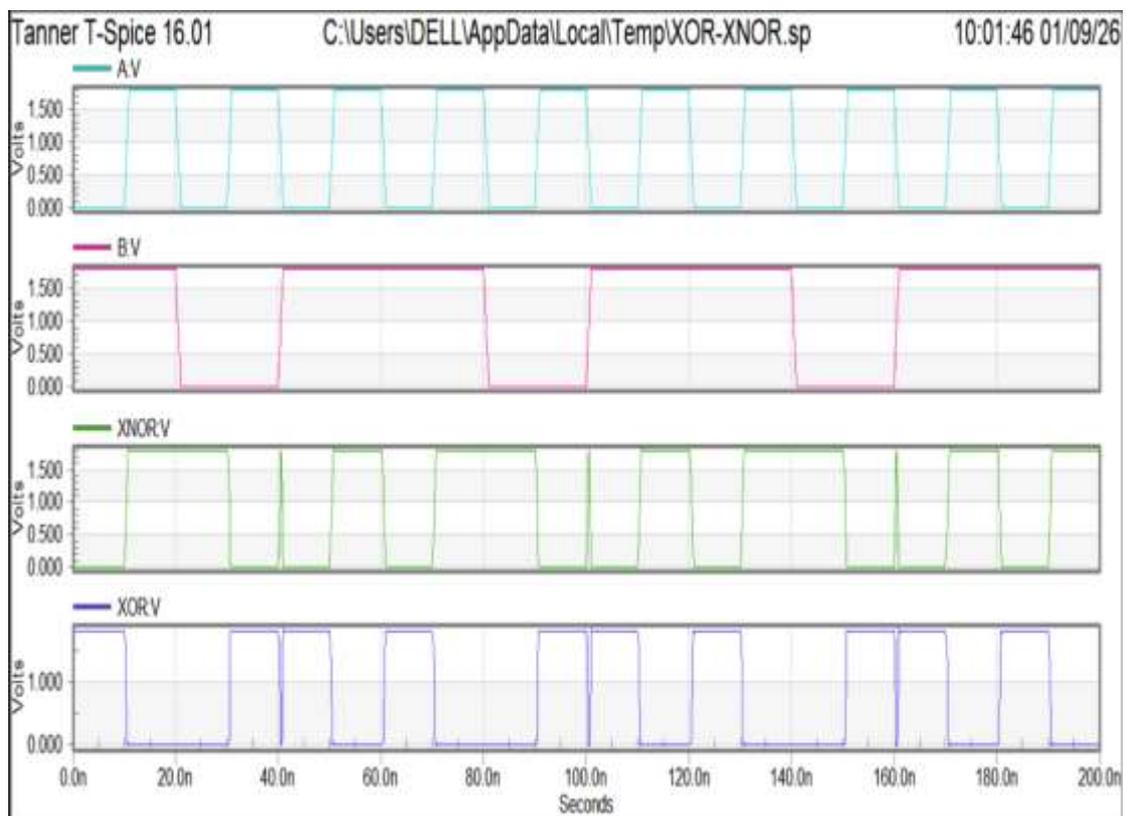


Fig 4: Xor/Xnoroutput

From the power analysis, the circuit consumes an average power of 5.44 μ W, indicating moderate power usage compared to a simple inverter due to higher transistor count and switching

activity. The maximum power ($\sim 352 \mu\text{W}$) occurs during input transitions because of short-circuit and dynamic power, while the minimum power ($\sim 51 \text{ nW}$) appears during steady logic states. Overall, the results validate correct functionality, proper complementary outputs, and acceptable low-power performance of the XOR–XNOR design.

```
Input file: conventional.sp
Progress: Simulation completed

Total nodes: 135      Active devices: 29      Independent sources: 0
Total devices: 33    Passive devices: 0      Controlled sources: 0

Total Power from time 0 to 1e-007
Average power consumed -> 2.006690e-006 watts
Max power 9.570817e-005 at time 4.1e-008
Min power 1.816153e-008 at time 5.13664e-008

Measure information will be written to file "C:\Users\DELL\AppData.

Measurement result summary
tp_sum_lh      = 192.4861p
tp_sum_hl      = 10.3917n
tp_car_lh      = 20.1763n
tp_car_hl      = 20.3811n
tp_sum_avg     = 5.2921n
tp_car_avg     = 20.2787n
tp_total       = 20.2787n
Pavg           = 2.0067u
PDP            = 40.6931f
EDP            = 825.2028e-024
```

Fig 5: conventional full adder Simulation

The simulation results show that the circuit has an average power consumption (P_{avg}) of $2.0067 \mu\text{W}$, indicating low power usage. The propagation delay (tp_{total}) is 20.2787 ns , with the Carry output being the critical path.

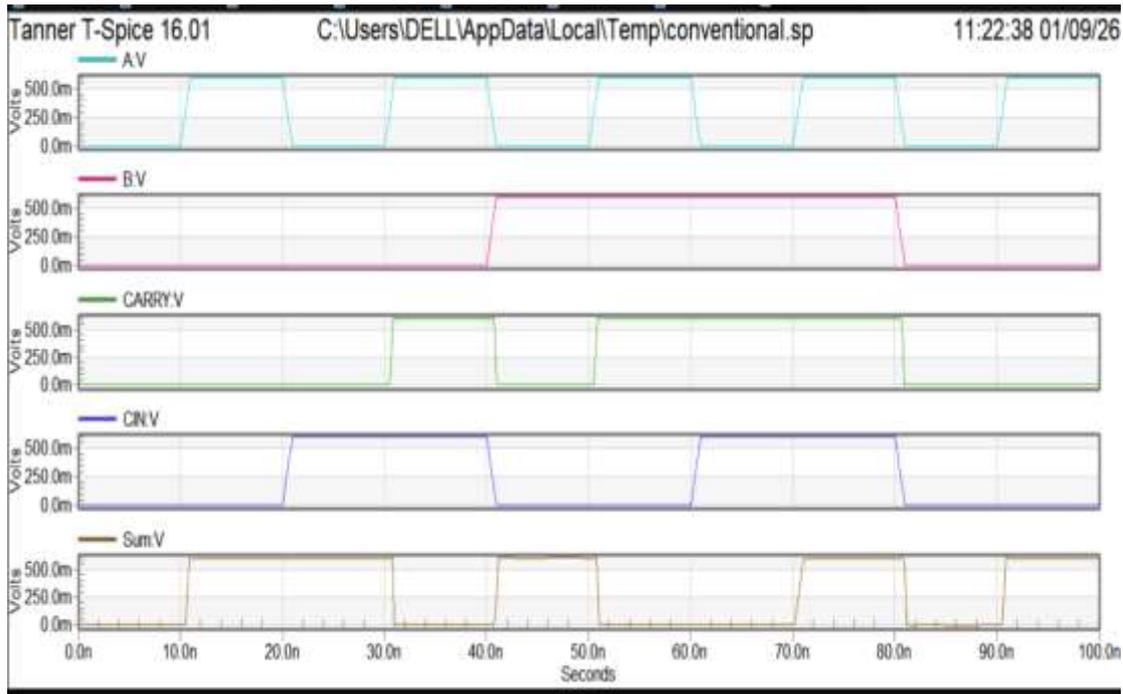


Fig 6: conventional full adder output

The Power-Delay Product (PDP) is 40.6931 fJ, and the Energy-Delay Product (EDP) is 825.2028 zJ, reflecting a good balance between speed and energy efficiency. Overall, these metrics indicate that the design is both fast and energy-efficient.

Input file:

Progress: Simulation completed

Total nodes:	94	Active devices:	20	Independent sources:	0
Total devices:	24	Passive devices:	0	Controlled sources:	0

```

Total Power from time 0 to 1e-007
Average power consumed -> 2.846689e-006 watts
Max power 1.484123e-004 at time 3.0875e-008
Min power 7.893174e-008 at time 0

Measure information will be written to file "C:\Users\DELL\AppData

Measurement result summary
tp_sum_lh      = 418.6651p
tp_sum_hl     = 10.3971n
tp_car_lh     = 119.2780p
tp_car_hl     = -9.6753n
tp_sum_avg    = 5.4079n
tp_car_avg    = -4.7780n
tp_total      = 5.4079n
Pavg          = 2.8467u
PDP           = 15.3945f
EDP           = 83.2514e-024
    
```

Fig 7: existing full adder Simulation

Figure 7 shows the transient simulation results of the existing full adder circuit obtained using Tanner T-Spice. The input waveforms (A, B, and CIN) are applied in different combinations, and the corresponding SUM and CARRY outputs follow correct full adder logic, confirming functional correctness. From the power analysis, the circuit consumes an average power of $2.8467 \mu\text{W}$, with a maximum instantaneous power of $1.484 \times 10^{-4} \text{ W}$. The measured propagation delay is in the nanosecond range ($t_{p_total} \approx 5.41 \text{ ns}$), indicating moderate speed performance. The Power-Delay Product (PDP) and Energy-Delay Product (EDP) values reflect a trade-off between power consumption and delay, showing that while the existing full adder operates reliably, it is not optimized for low-power or high-speed operation compared to reduced-transistor or voltage-resilient designs.

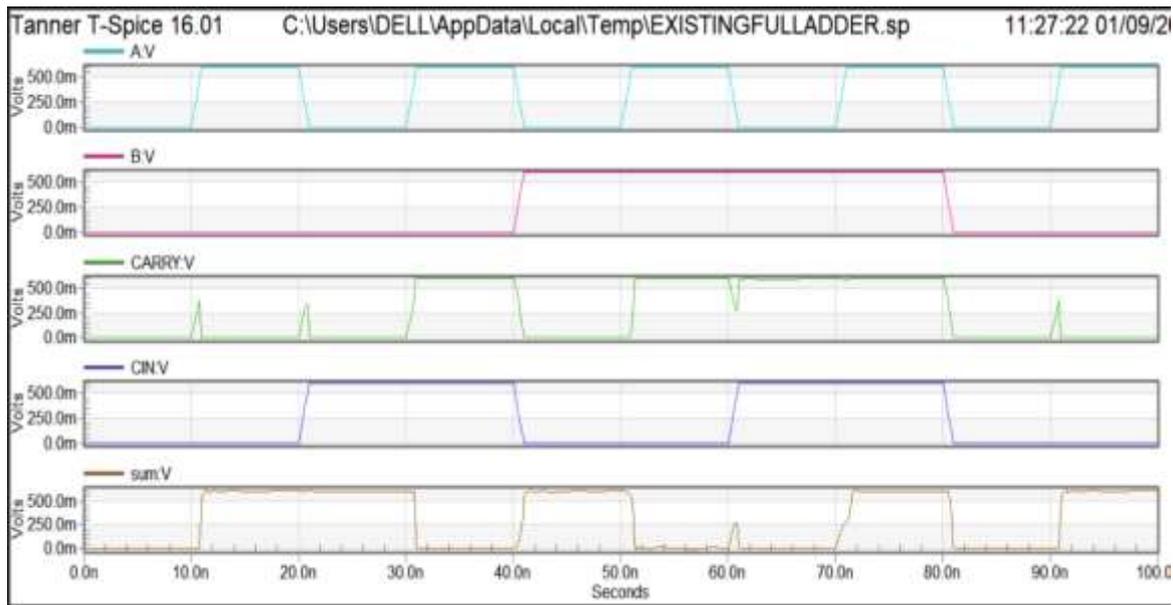


Fig 8: conventional full adder output

Below fig presents the transient simulation results of the proposed full adder circuit using Tanner T-Spice. The input signals (A, B, and CIN) are applied in all combinations, and the SUM and CARRY waveforms clearly follow the correct full adder logic, demonstrating proper functionality. Compared to the existing design, the proposed full adder shows a reduced device count and improved performance. The average power consumption is $2.5997 \mu\text{W}$, which is lower than that of the existing full adder, indicating better power efficiency. The total propagation delay is approximately 5.39 ns , showing comparable or slightly improved speed. Furthermore, the reduced PDP (14.02 fJ) and EDP (75.65×10^{-24}) highlight the energy-efficient nature of the proposed design, making it more suitable for low-power and high-performance VLSI applications.

In extension to the existing full adder simulation results, the proposed full adder demonstrates clear improvements in both power and energy efficiency while maintaining correct functionality. The transient waveforms show that the SUM and CARRY outputs closely follow the input combinations of A, B, and CIN with stable voltage levels and reduced glitches. Owing to the reduced transistor count, the average power consumption is lowered to $2.5997 \mu\text{W}$, and the total propagation delay remains comparable at approximately 5.39 ns . The noticeable reduction in PDP and EDP further indicates that the proposed design achieves better energy-delay trade-off, making it more suitable for low-power, high-performance arithmetic units compared to the existing full adder.

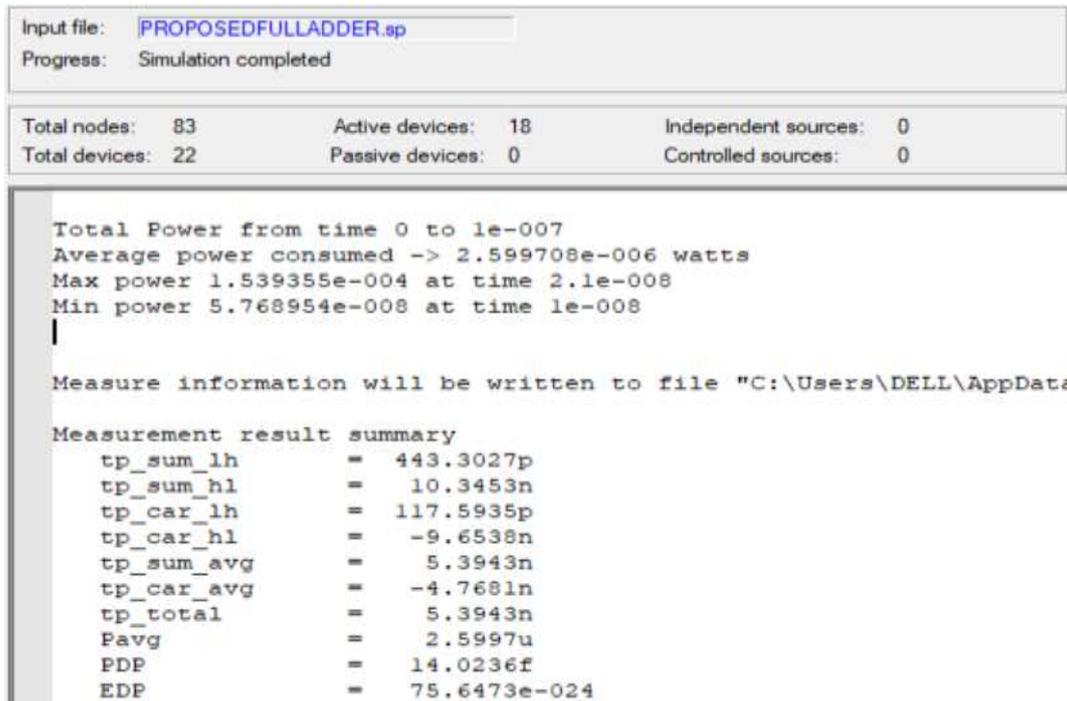


Fig 9 :proposed full adder Simulation

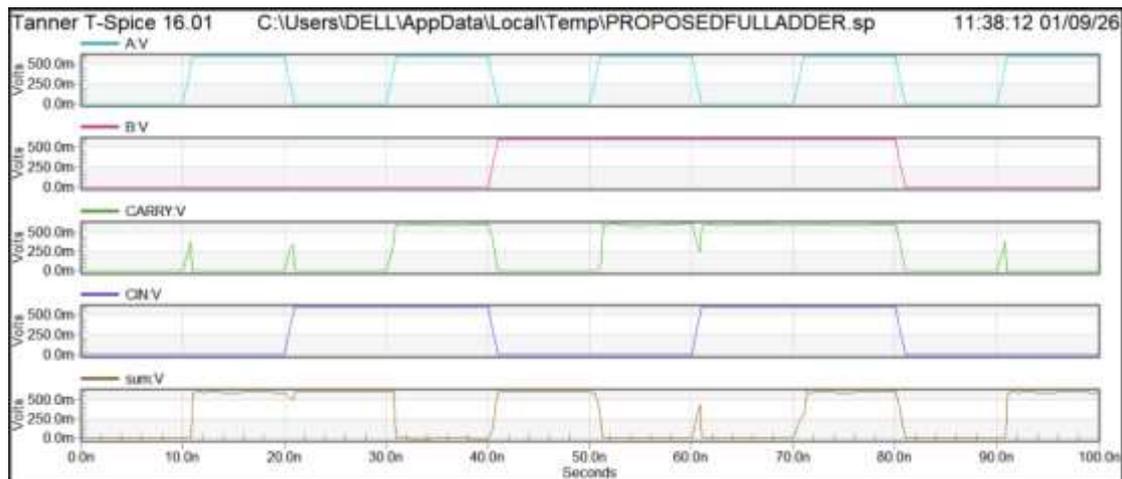


Fig 10: proposed full adder output

VI CONCLUSION

This work presents the design and comprehensive evaluation of a voltage-resilient Static Adaptive Energy (SAE) keeper-based full adder implemented using 90-nm CMOS technology and simulated in Tanner T-Spice. The proposed architecture focuses on reducing transistor count while maintaining full voltage swing, low power consumption, and high-speed operation. Comparative analysis with conventional and existing full adder designs confirms that the proposed 16-transistor structure achieves improved energy efficiency without compromising functional correctness. Simulation results demonstrate reduced average power consumption, competitive propagation delay, and significantly improved Power–Delay Product (PDP) and Energy–Delay Product (EDP), indicating a superior trade-off between speed and energy performance. The incorporation of a grounded keeper mechanism effectively restores degraded voltage levels and enhances noise immunity under scaled supply voltages. Stable SUM and CARRY outputs across all input combinations validate the

robustness of the design. Furthermore, the proposed full adder proves suitable for integration into ripple carry adders and larger arithmetic systems. Overall, the presented transistor-level optimization strategy provides a practical solution for developing reliable, low-power, and high-performance arithmetic circuits in modern VLSI applications.

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