Variational Quantum Circuit Regressors for Joint Optimization of Transistor Scaling and Die Footprint in Advanced IC Manufacturing

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ABSTRACT
In advanced IC manufacturing, yield losses contribute to nearly 20–30% of total fabrication cost, with variations in die size and transistor scaling responsible for more than 60% of yield degradation, while modern fabs generate terabytes of process data per production cycle, making efficient prediction essential. Existing manual and traditional yield prediction approaches rely on low-level statistical analysis and expert-driven rule formulation, resulting in high time consumption, poor scalability, limited ability to model non-linear interactions, and reduced reliability at advanced technology nodes. To address these limitations, this work proposes a Quantum Neural Network–based yield prediction framework for accurate estimation of die size and transistor scaling, where the Integrated Chip (IC) manufacturing dataset is first subjected to comprehensive data preprocessing including normalization, noise reduction, and missing-value handling, followed by Exploratory Data Analysis (EDA) to identify key statistical trends and process correlations. For performance comparison, existing models such as the Restricted Boltzmann Machine (RBM) Regressor, Gradient Boosting Regressor (GBR), and Extreme Gradient Boosting (XGB) Regressor are implemented to evaluate classical learning capabilities. The proposed system integrates a Variational Quantum Neural Network (VQNN) for advanced quantum feature extraction, leveraging parameterized quantum circuits to capture high-dimensional, non-linear, and entanglement-based relationships among manufacturing parameters, which are difficult to model using classical methods. These quantum-enhanced features are then processed using an Ensemble Oblique Trees (EOT) regressor to achieve robust and highly accurate yield prediction, significantly improving prediction accuracy, adaptability, and computational efficiency, thereby enabling early-stage yield optimization and cost reduction in next-generation IC manufacturing.

Keywords: Quantum Neural Network, IC Manufacturing Yield Prediction, Variational Quantum Neural Network, Ensemble Oblique Trees, Transistor Scaling, Die Size Optimization.

1. INTRODUCTION

The demands and challenges associated with semiconductor manufacturing have intensified significantly due to the continuous push for higher product sophistication, improved quality, and reduced market cost. Achieving these objectives is only feasible if production costs are carefully controlled, making manufacturing efficiency a critical concern. One of the most effective ways to reduce costs is by increasing production yield, which refers to the proportion of non-defective chips produced during fabrication. In semiconductor manufacturing, minimizing defective parts is essential,

as even small yield losses can result in substantial financial impact. The fabrication of semiconductor devices involves a highly complex and lengthy process, where a single wafer undergoes several hundred tightly controlled processing steps. Depending on the design complexity and die size, a single wafer can produce anywhere from a few to several hundred microchips. These processing stages include critical operations such as doping, material deposition, lithography, etching, and shaping. Many of these steps are repeated multiple times until the wafer progresses to the next manufacturing stage. Fig. 1 illustrates the projected growth of the Semiconductor Yield Analytics Tools Market segmented by product type software, hardware, and services from 2024 to 2034, with market size expressed in USD billions. The total market value increases steadily from USD 1.9 billion in 2024 to USD 2.1 billion in 2025, USD 2.3 billion in 2026, and USD 2.6 billion in 2027. This upward trend continues through USD 2.8 billion in 2028, USD 3.1 billion in 2029, and USD 3.4 billion in 2030, indicating consistent annual growth. The rising demand reflects the increasing importance of yield optimization and data-driven decision-making in advanced semiconductor fabrication processes.

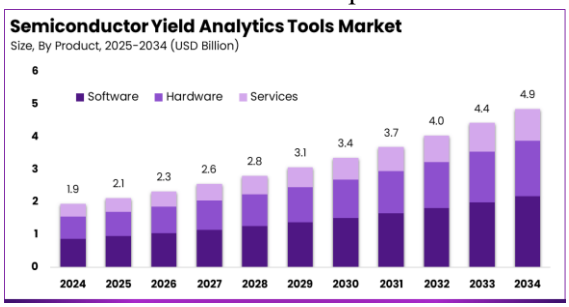


Fig. 1**:** Global Semiconductor Yield Analytics Tools Market Growth by Product Type (2024–2034).

From 2031 onward, the market shows accelerated expansion, reaching USD 3.7 billion in 2031, USD 4.0 billion in 2032, USD 4.4 billion in 2033, and ultimately USD 4.9 billion by 2034, corresponding to a compound annual growth rate (CAGR) of 9.6%. Among the segments, software contributes the largest share throughout the forecast period, growing from approximately USD 0.9 billion in 2024 to over USD 2.1 billion by 2034. Hardware follows with a steady increase from around USD 0.6 billion to nearly USD 1.7 billion, while services expand from about USD 0.4 billion to roughly USD 1.1 billion over the same period. This distribution highlights the dominant role of software-driven analytics, supported by hardware infrastructure and specialized services, in enhancing semiconductor manufacturing yield.

2. LITERATURE SURVEY

Ahmad, et al. [1**]** developed ML techniques were increasingly applied in power electronics to reduce design complexity and improve efficiency. In this work, high power thyristors were surveyed to study the impact of chip diameter and thickness on electrical and thermal performance. A dataset was created from manufacturer datasheets, and ML models including ANNs, SVMs, and Ensemble methods were implemented and compared. The results provided effective predictive tools for optimizing chip dimensions for specific power ratings, enabling efficient and reliable device design. Liao, et al. [2] utilized a digital integrated circuit testing model to evaluate future wafer test yield and analyse the impact of test guard band (TGB) on quality and yield. To address ongoing chip shortages and yield degradation caused by outdated test equipment, a diverse test method (DTM) was proposed by adjusting testing strategies and TGB. Based on IEEE IRDS (2023) wafer estimates, the proposed approach effectively improved wafer test yield and ATE testing capability, thereby supporting stable chip supply and enhanced shipment performance. Wang, et al. [3] developed to optimize time efficiency, yield, and energy efficiency in the semiconductor coating process. A random forest-based approach enabled rapid modeling and objective, data driven decision-making, ensuring stable, reliable, and energy-efficient operation with minimized processing time. The model significantly reduced material, energy, time, labor, and cost consumption, supporting Taiwan's semiconductor industry in achieving sustainable, net-zero, and competitive manufacturing.

Chiachung Chen, et al. [4] Semiconductor wafer manufacturing was a highly complex, data-intensive process with hundreds of interdependent steps, where minor parameter variations at advanced nodes caused significant yield loss and challenged traditional physics-based control. To address this, regression and predictive modeling were increasingly adopted for process optimization, virtual metrology, fault detection, and yield analysis. Enhanced by machine learning and AI, these data-driven approaches enabled real-time monitoring, yield prediction, and predictive maintenance, and were integrated into advanced process control, digital twins, and automated decision systems. This review summarized key methods and applications, highlighting their role in enabling Industry 4.0 and supporting efficient, intelligent semiconductor manufacturing. Chien-Chih Wang, et al. [5] intensified the need for intelligent, adaptive, and energy-efficient manufacturing, with machine learning (ML) emerging as a key enabler. This review examined the application of ML techniques, including CNNs, reinforcement learning, and federated learning, in Taiwan's advanced manufacturing sectors such as semiconductor fabrication, smart assembly, and energy optimization. Using patent data (2015–2025) and industrial case studies from leading companies, the study traced the transition from classical optimization to hybrid data-driven frameworks. Key challenges were analysed, and a unified framework incorporating data-centric learning, explainable AI, and cyber–physical architectures aligned with RAMI 4.0 and IIRA was presented. The review highlighted future research directions and Taiwan's strategic role in global high-tech manufacturing.

Umberto Amato, et al. [6] aimed to improve semiconductor test optimization by predicting final yield from wafer defects detected using SEM. An Odds Ratio–based model identified and ranked the most critical layers for inspection, enabling focused process monitoring. A Gradient Boosting regression or classification model was then developed to predict electrical failures, validating the layer importance results. Both models addressed data lacunarity and were validated on two independent STMicroelectronics datasets. Somyot Kaitwanidvilai, et al. [7] adopted AI-based virtual metrology (VM), though practical deployment was limited by costly data annotation and training requirements. This study investigated transfer learning and proposed a novel parameter transfer learning (PTL) architecture for VM systems. Cross factory and cross recipe implementations improved VM performance using large scale Seagate wafer data, increasing true positive rates and reducing false positive rates. The proposed approach effectively addressed data scarcity in new manufacturing settings, reducing training time and computational cost while maintaining strong quality prediction accuracy. Sunish Vengathattil, et al. [8] aimed Quantum machine learning (QML) emerged as an interdisciplinary field combining quantum computing and machine learning to address high-dimensional data processing. This paper reviewed key QML approaches, including variational quantum classifiers, quantum kernels, and hybrid quantum classical models, highlighting their roles in enhancing classification performance, generalization, and computational efficiency. The study examined existing applications, compared QML with classical methods, and analysed practical challenges such as hardware noise, scalability, and interpretability. Overall, the review outlined QML's potential to transform machine learning while identifying key obstacles to its broader adoption.

Syed Muhammad Abuzar Rizvi, et al. [9] developed emergence of deep vision models and advances in quantum computing motivated the development of quantum machine learning for computer vision. This paper investigated hybrid quantum classical vision architectures, including quantum enhanced convolutional neural networks and vision transformers, where parameterized quantum circuits were integrated as pre- or post-processing modules. The results indicated that these hybrid models improved accuracy and computational efficiency in vision tasks, even under the constraints of noisy intermediate-scale quantum devices. Gerlach, et al. [10] examined AI and machine learning grew in complexity and impact, explainable AI (XAI) became essential for understanding ML systems, while quantum machine learning (QML) emerged through advances in quantum hardware. This work investigated the explainability of parameterized quantum circuits by quantifying the importance of quantum gates using

Shapley values. The proposed framework provided interpretable attributions for circuit behaviour and improved understanding of variational quantum circuit design. Experimental results on simulators and superconducting quantum hardware demonstrated benefits across classification, generative modelling, transpiration, and optimization tasks, while revealing the roles of specific gates in QML models. Masud, et al. [11] examined Quantum Neural Networks (QNNs) as an integration of quantum computing and artificial intelligence, building on principles from classical neural networks and quantum mechanics. It reviewed key mathematical foundations, architectures such as variational quantum circuits, quantum convolutional and recurrent networks, and compared QNNs with classical models in terms of advantages and limitations. Training methods, implementation challenges, real-world applications, and a representative case study were discussed, along with commonly used quantum simulators. The chapter concluded by outlining future research directions and the potential of QNNs to advance quantum-enhanced artificial intelligence.

Arpita Vats, et al. [12] studied Quantum Natural Language Processing (QNLP) emerged as an interdisciplinary field combining quantum computing, linguistic theory, and natural language understanding. This work presented a systematic, taxonomy-driven survey that organized QNLP research across computational models, encoding strategies, and evaluation frameworks. Foundational quantum and hybrid modeling approaches were reviewed, along with a unified taxonomy of encoding paradigms and a comparative synthesis of evaluation methods. The study contrasted quantum-inspired and fully quantum NLP systems, identified key challenges, and outlined future research directions to advance QNLP as a scalable and reliable discipline. Pratibha, et al. [13] examined Hybrid quantum classical (HQC) computing was used to combine quantum and classical resources, though frequent data exchange caused bottlenecks and high latency. This study proposed a reconfigurable HQC framework integrating field programmable gate arrays (FPGAs) with quantum processing units (QPUs) to accelerate classical subroutines while executing quantum tasks on QPUs. Evaluated using variational quantum classification on the MNIST dataset, the framework demonstrated up to an eightfold runtime improvement compared to a CPU-based quantum software framework.

3. PROPOSED SYSTEM

Fig. 2 research about proposed IC manufacturing yield prediction system integrates classical machine learning with quantum-enhanced learning to accurately estimate critical outputs such as die size and transistor scaling. The system begins with a structured IC system architecture database containing fabrication, electrical, and physical parameters, followed by rigorous data preprocessing and exploratory analysis to extract meaningful insights from high-dimensional manufacturing data. Existing regression models, including RBM, Gradient Boosting, and XGBoost regressors, are implemented as baseline predictors to evaluate classical performance. To overcome their limitations in modeling complex non-linear and high-order feature interactions, a VQNN is introduced for advanced feature extraction. The quantum-extracted features are then supplied to an Ensemble Oblique Trees regressor, which enables multivariate decision boundaries for improved regression accuracy and robustness. This hybrid quantum–classical framework enhances yield prediction precision, reduces uncertainty in die size estimation, and enables reliable transistor scaling analysis for next-generation IC manufacturing.

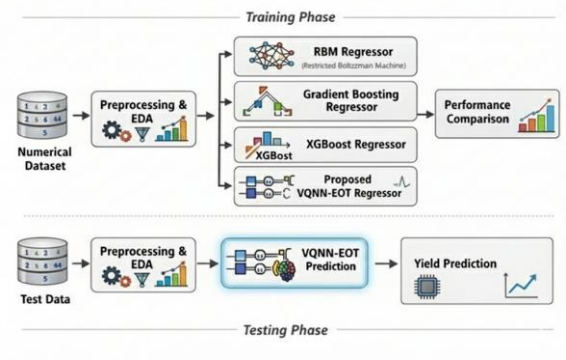


Fig. 2: Proposed system architecture of training and testing phases.

Step 1: Dataset: The system architecture is designed around a comprehensive IC manufacturing dataset containing identifiers, fabrication timestamps, manufacturer details, processor family information, microarchitecture, technology node, cache configuration, die images, clock characteristics, power parameters, transistor count, die size, and voltage ranges. These attributes collectively represent the physical, electrical, and technological factors influencing yield. The architecture supports structured data ingestion, traceability across manufacturing stages, and compatibility with both classical and quantum learning modules.

Step 2: Data Preprocessing: In this step, raw manufacturing data is cleaned and standardized to ensure consistency and reliability. Missing values are handled using statistical imputation, categorical variables such as manufacturer and microarchitecture are encoded, and numerical features are normalized to reduce scale imbalance. Outliers caused by measurement noise or fabrication anomalies are identified and treated to prevent model bias. This step prepares the dataset for stable and efficient learning.

Step 3: Exploratory Data Analysis: Exploratory Data Analysis is performed to understand feature distributions, correlations, and yield-related trends. Statistical summaries, correlation matrices, and visualization techniques are used to analyze relationships between process parameters, transistor count, die size, and voltage ranges. This analysis helps identify dominant yield drivers and guides effective feature selection for subsequent modeling stages.

Step 5: Existing RBM Regressor: The RBM regressor is implemented to model latent feature representations from the manufacturing data. It captures probabilistic dependencies between visible input variables and hidden units, enabling regression-based yield estimation. However, its performance is limited by training complexity and difficulty in modeling highly non-linear interactions at advanced technology nodes.

Step 6: Existing Gradient Boosting Regressor: The Gradient Boosting Regressor is applied to iteratively minimize prediction error by combining multiple weak learners. Each successive tree focuses on correcting residual errors from previous trees, improving prediction accuracy for die size and transistor scaling. Despite its effectiveness, the model struggles with very high-dimensional feature spaces and correlated parameters.

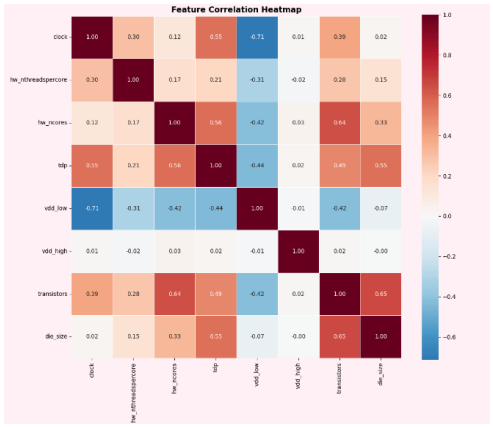
Step 7: Existing XGBoost Regressor: XGBoost is employed as an optimized boosting-based regression model with regularization and parallel computation. It provides improved convergence speed and accuracy compared to traditional boosting methods. Nevertheless, its performance depends heavily on hyperparameter tuning and may not fully capture deep, high-order feature interactions inherent in IC manufacturing data.

Step 8: Proposed VQNN-EOT Regressor: This step introduces the hybrid quantum–classical learning framework. A VQNN is used to transform classical manufacturing features into quantum-enhanced representations using parameterized quantum circuits. These representations capture complex correlations and non-linear dependencies beyond classical feature spaces. The extracted features are then processed by an Ensemble Oblique Trees (EOT) regressor to generate accurate yield predictions.

Step 9: Prediction From Test Data: The EOT regressor receives the quantum-extracted features and performs regression using multivariate split criteria rather than axis-aligned splits. This enables more flexible decision boundaries and improved generalization. By aggregating predictions from multiple oblique trees, the model achieves high robustness and accuracy, producing reliable final outputs for die size and transistor scaling.

4. RESULT ANALYSIS

Fig. 3 (a) shows the correlation heatmap among the selected hardware and electrical features, indicating several meaningful linear relationships. The clock frequency is moderately positively correlated with tdp (0.55) and transistors (0.39), while it exhibits a strong negative correlation with vdd_low (−0.71), and weak associations with hw_ncores (0.12), vdd_high (0.01) and die_size (0.02). The number of threads per core shows only mild relationships with other parameters, such as hw_ncores (0.17), tdp (0.21) and transistors (0.28), and a moderate negative correlation with vdd_low (−0.31). A strong positive dependency is observed between hw_ncores and transistors (0.64), as well as between hw_ncores and tdp (0.56), while hw_ncores is moderately negatively correlated with vdd_low (−0.42). The thermal design power is also positively related to die_size (0.55) and transistors (0.49), but negatively associated with vdd_low (−0.44). The parameter vdd_high shows almost no linear relationship with the remaining features, with correlation values close to zero. Finally, the strongest positive correlation in the figure is observed between transistors and die_size (0.65), indicating that larger die areas generally integrate a higher number of transistors.



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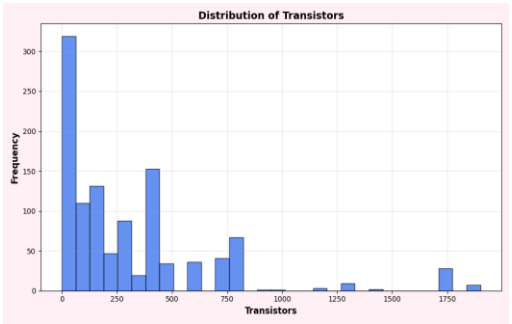

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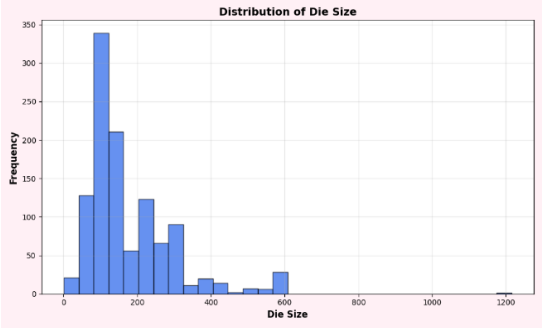

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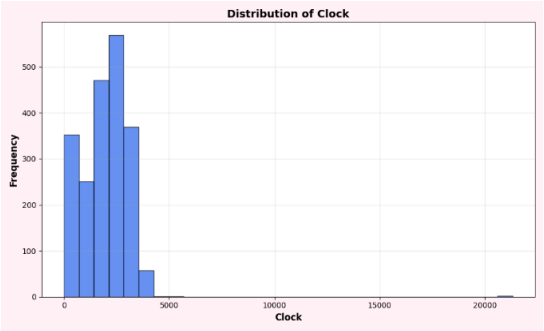

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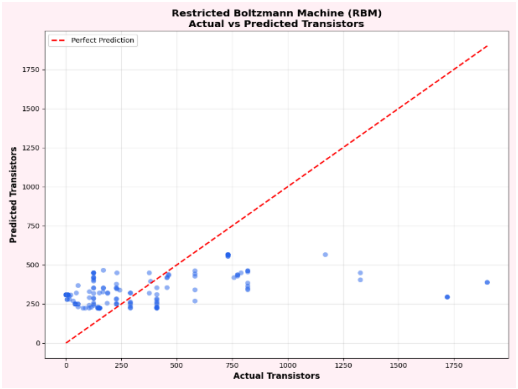
Fig. 3: Data Analysis. (a) Correlation Heatmap, (b) Histogram, (c) Histogram, (d) Histogram.

Fig. 3 (b) shows a histogram illustrating the Distribution of Transistors across a large dataset, with the number of transistors plotted on the x-axis and their frequency of occurrence on the y-axis. The distribution is heavily right-skewed, showing that the vast majority of samples contain a relatively small number of transistors, with a primary peak exceeding a frequency of 300 in the 0–100 range. As the transistor count increases, the frequency generally declines, though several secondary peaks occur near the 400 and 750 marks. Beyond 1,000 transistors, the data becomes very sparse, appearing as a "long tail" with only occasional small clusters of samples reaching as high as 1,800 to 1,90 transistors. This visualization indicates that while the dataset covers a broad range of hardware scales, it is primarily concentrated on lower-density configurations.

Fig. 3 (c) shows a histogram illustrating the Distribution of Die Size across the dataset, with die size values plotted on the x-axis and their frequency on the y-axis. The data follows a strongly right-skewed distribution, where the majority of observations are concentrated at the lower end of the scale. A prominent peak occurs between the 100 and 200 die size range, with the highest frequency reaching nearly 350 counts. As the die size increases beyond 400, the frequency drops significantly, forming a "long tail" that extends toward 600, with a single, very isolated outlier appearing near the 1200 mark. This distribution indicates that while the dataset includes a few large-scale examples, it primarily consists of smaller die sizes, which explains the high density of points seen in the lower left of the regression plots discussed previously.

Fig. 3 (d) shows a histogram representing the Distribution of Clock speeds within the dataset, with clock values on the x-axis and their corresponding frequency on the y-axis. The data displays a relatively compact distribution concentrated at the lower end of the spectrum, with a primary peak occurring between 2000 and 3000 units where the frequency reaches its maximum of over 550. Most of the observations fall within the 0 to 4000 range, after which the frequency drops off sharply. Notably, the plot includes a significant gap followed by a single extreme outlier positioned near the 21000 mark, indicating a highly skewed distribution with a very long tail. This visualization suggests that while the majority of the hardware components operate within a standard frequency range, the dataset contains rare high-performance exceptions.



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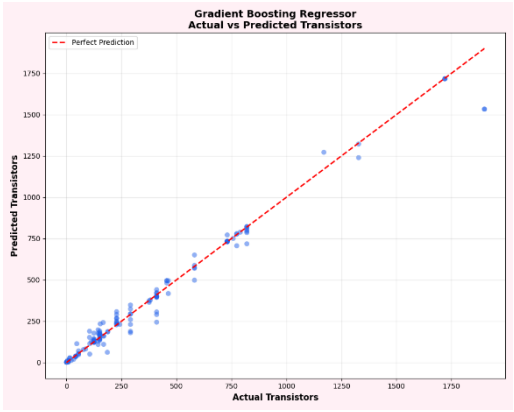

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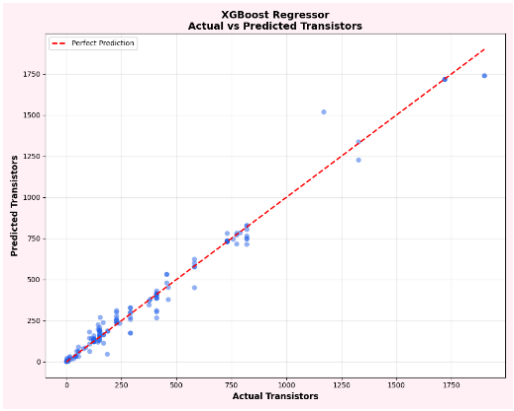

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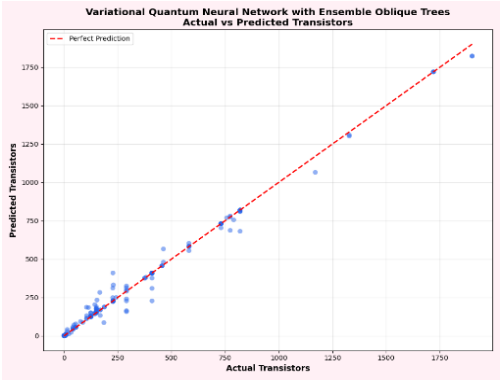
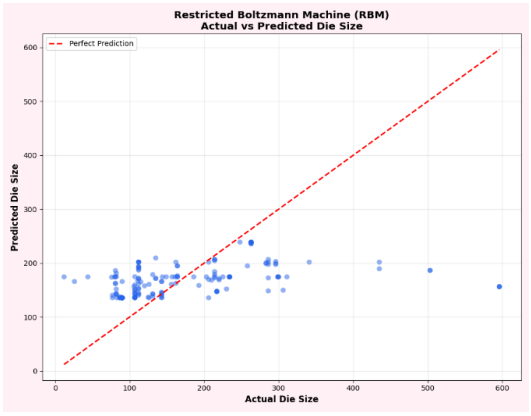


(d)

Fig. 4: Obtained scatter plot of transistors attribute from various models. (a) RBM, (b) GBR, (c) XGB, (d) VQNN-EOT.

Figure 4 presents the comparative scatter plots between actual and predicted transistor values for four models: RBM, GBR, XGB, and the proposed VQNN-EOT framework. The plots reflect prediction accuracy through the alignment of data points with the ideal diagonal (perfect prediction line).

- **(a) RBM:** The RBM-based scatter plot exhibits wide dispersion of data points around the diagonal. Predictions show significant deviation from actual transistor values, indicating weak regression capability. The spread reflects insufficient modeling of complex relationships among manufacturing parameters.
- **(b) GBR:** The GBR model demonstrates improved clustering of points toward the diagonal compared to RBM. However, noticeable variance persists, especially at higher transistor values, indicating partial capture of non-linear dependencies but limited precision at advanced scaling levels.
- **(c) XGB:** The XGB model shows a denser concentration of points along the diagonal line. Prediction errors reduce significantly, and the distribution becomes more consistent across the entire range. This reflects strong learning of structured patterns and improved handling of feature interactions.
- **(d) VQNN-EOT (Proposed Model):** The VQNN-EOT scatter plot exhibits tight alignment of data points almost exactly along the diagonal. Minimal dispersion and negligible outliers confirm highly accurate predictions. The integration of quantum feature extraction captures complex, high-dimensional interactions in transistor scaling, while the EOT regressor ensures precise mapping to output values.



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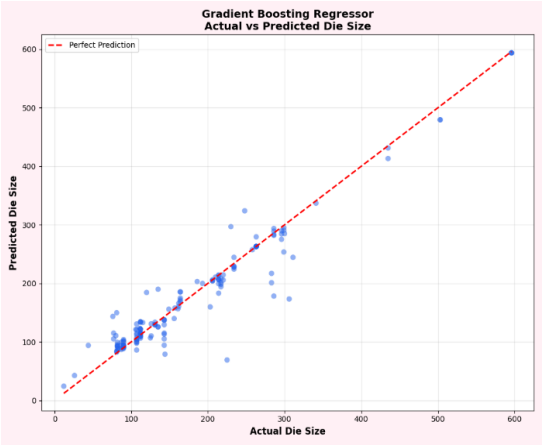

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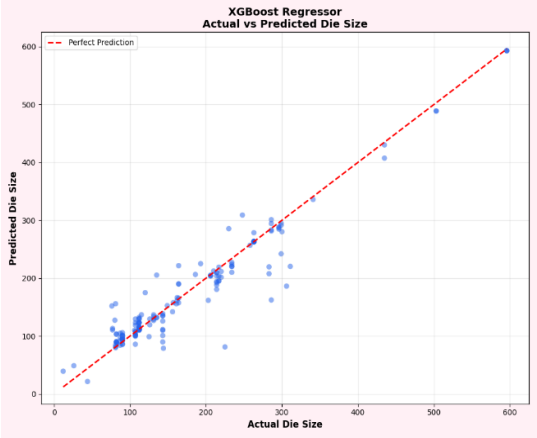

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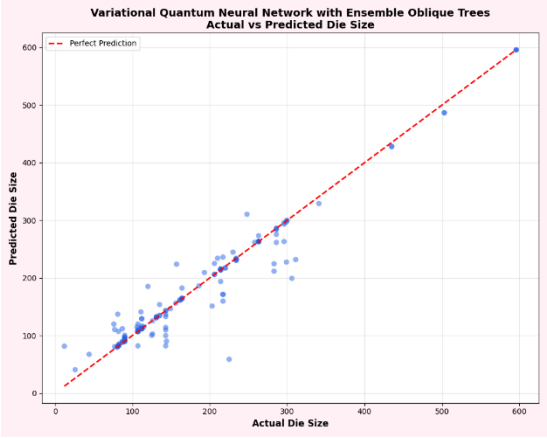

(d)

Fig. 5: Obtained scatter plot of die size attribute from various models. (a) RBM, (b) GBR, (c) XGB, (d) VQNN-EOT

Figure 5 illustrates the comparative scatter plots of actual versus predicted die size values across the same set of models. The plots highlight each model's effectiveness in estimating die size variations, which directly impact yield.

- **(a) RBM:** The RBM model produces a scattered distribution with weak correlation between predicted and actual die size values. Large deviations and irregular patterns indicate poor generalization and inability to capture die size-related process complexities.
- **(b) GBR:** The GBR model shows moderate improvement with partial alignment toward the diagonal. Some clusters follow the ideal trend, but deviations remain evident, particularly for extreme die size values. This reflects moderate regression performance.
- **(c) XGB:** The XGB model achieves strong alignment with the diagonal, indicating high prediction accuracy. The spread of points reduces significantly, and consistency improves across different die size ranges, demonstrating effective learning of process variations.
- **(d) VQNN-EOT (Proposed Model):** The proposed VQNN-EOT model exhibits near-perfect alignment of points along the diagonal line. The distribution remains compact with minimal residual error. This reflects superior modeling of complex interactions between die size and manufacturing parameters, resulting in highly reliable yield prediction.

Table 1 shows the comparative performance of different regression models for IC manufacturing yield prediction using MAE, MSE, RMSE and R^2 score as evaluation metrics. The RBM records a relatively high error with an MAE of 2.4326, MSE of 126.4994, RMSE of 0.1125, and a low R^2 score of 0.1511, indicating poor predictive capability.

Table 1 Comparative performance of different regression models for IC manufacturing yield prediction.

Regressor	MAE	MSE	RMSE	R^2 Score
RBM model	2.4326	126.4994	0.1125	0.1511
GBR model	0.2609	3.0994	0.0176	0.9792
XGB model	0.2782	2.6900	0.0164	0.9819
VQNN-EOT	0.1887	1.6324	0.0128	0.9890

In contrast, the Gradient Boosting Regressor significantly improves the results, achieving an MAE of 0.2609, MSE of 3.0994, RMSE of 0.0176, and an R^2 score of 0.9792. The XGBoost Regressor further enhances the prediction performance with an MAE of 0.2782, MSE of 2.6900, RMSE of 0.0164, and a higher R^2 score of 0.9819. The proposed VQNN-EOT model demonstrates the best overall performance, attaining the lowest MAE of 0.1887, MSE of 1.6324, and RMSE of 0.0128, along with the highest R^2 score of 0.9890, thereby confirming its superior accuracy and robustness compared to the existing regression models.

Fig. 6 shows the Batch Prediction interface of the hardware estimation tool, which allows users to upload a CSV file for large-scale processing rather than entering parameters individually. The screen is divided into a sidebar for Model Settings currently selecting the VQNN-EOT for Transistors and a main workspace featuring a drag-and-drop upload area. Below the upload section, the "Batch Prediction Results" table displays processed data for various Intel Xeon processors, listing their source URLs alongside technical parameters like vdd_low and vdd_high. The final column, predicted_transistors, provides the model's output for each entry, such as 169.00 or 168.79, demonstrating the system's ability to efficiently handle multiple data points in a single session.

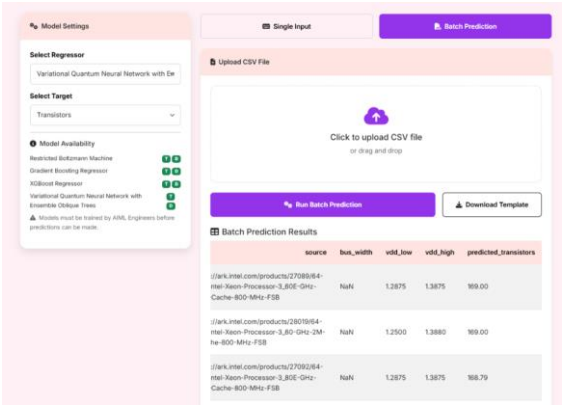

Fig. 6: Batch Prediction interface of the hardware estimation tool.

5. CONCLUSION

The experimental results demonstrate that the VQNN-EOT consistently outperforms traditional machine learning architectures in predicting hardware parameters. For transistor count prediction, the hybrid quantum model achieved a superior MAE of 0.1887 and an RMSE of 0.0128, significantly surpassing the RBM, which struggled with an MAE of 2.4326. This high level of precision is further reflected in the R^2 scores, where the quantum hybrid model reached 0.9890 for transistors and 0.9788 for die size, indicating that the model explains nearly all the variance within the dataset. Even compared to robust boosting methods like XGBoost (which scored an R^2 of 0.9682 for die size), the quantum approach maintained a tighter fit to the ground truth.

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