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EFFICIENT VLSI ARCHITECTURE FOR OTFS MODULATION WITH ZERO-FORCING EQUALIZATION

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ABSTRACT

Orthogonal Time Frequency Space (OTFS) modulation is a promising technique known for its robustness in time-varying channels, making it well-suited for high-mobility communication environments. This project focuses on the design and hardware implementation of a low-complexity Zero Forcing (ZF) equalizer for a Single-Input Single-Output (SISO) OTFS system. To reduce computational complexity and hardware overhead, we propose a Very Large Scale Integration (VLSI) architecture that incorporates parallel processing and resource optimization techniques. A key feature of the design is the use of a back-to-back Fast Fourier Transform (FFT) and Inverse FFT (IFFT) structure, which simplifies matrix inversion operations and allows for efficient updates without significantly degrading performance. The architecture is carefully crafted to support real-time processing while satisfying area and latency requirements. Through extensive simulations and evaluations, we study the trade-offs between reduced complexity and equalization performance. Performance metrics such as Bit Error Rate (BER), latency, and hardware area are used to evaluate the design. Synthesis results on a Xilinx 7vx485tffg1157-1 FPGA demonstrate the effectiveness of the proposed architecture, achieving a latency of 440 ns at a 100 MHz clock frequency, utilizing 249,843 Look-Up Tables (LUTs) and 74,611 Flip-Flops (FFs).

Keywords: Zero Forcing Equalizer, Orthogonal Time Frequency Space (OTFS), FFT/IFFT-Based Processing, Low-Complexity Equalization.

1. INTRODUCTION

Real-time mobile communications refer to the instantaneous exchange of voice, video, and data over wireless networks. These communications are critical for personal, business, and industrial applications, enabling seamless connectivity anywhere, anytime. Real-time communication systems refer to technologies and platforms that allow users to communicate and exchange information in real time, with minimal latency. These systems are designed to ensure that data is transmitted without noticeable delays, making them crucial for applications such as video conferencing, online gaming, voice calls, and live streaming. Key features of real-time communication systems include low latency, high availability, scalability, and seamless integration with different devices and platforms. One of the most common examples of real-time communication is Voice over IP (VoIP), where voice data is

transmitted over the internet, enabling real-time voice calls. In addition to voice, video communication tools like Zoom and Skype enable individuals and organizations to hold face-to-face meetings remotely. These systems rely on complex algorithms for compression, encryption, and error correction to maintain high-quality communication while keeping delays to a minimum. Security and privacy are critical considerations in real-time communication systems. With the increasing amount of sensitive information being shared during real-time interactions, encryption protocols like Secure Real-Time Transport Protocol (SRTP) and Transport Layer Security (TLS) are used to protect data from unauthorized access. Additionally, real-time communication systems must also address issues like network congestion, packet loss, and jitter to ensure smooth and reliable interactions, making Quality of Service (QoS) and adaptive streaming essential components of these systems.

2. LITERATURE SURVEY

Wu et al. [1] Wu and colleagues in their 2009 work focused on the design of a high- speed Quadrature Phase Shift Keying (QPSK) modulator using VLSI techniques. Their approach utilized a pipelined architecture to enable faster data processing with minimal latency, a critical aspect for high-performance wireless communication. The pipelined structure allowed for multiple operations to be executed concurrently, enhancing the throughput of the system without increasing power consumption. The study's primary observation was that by using pipelined stages, the speed of the modulator could be significantly improved, making it suitable for high-speed wireless communication applications, while also minimizing power consumption and area.

Sullivan et al. [2] Sullivan et al. (2010) made strides in the design of high-speed VLSI modulators and demodulators specifically for 4G LTE wireless communication systems. They focused on achieving ultra-low latency and high throughput, both of which are critical for real- time communication systems. Their approach involved using pipelined architectures and parallel processing techniques to enhance performance. The main observation was that high- speed digital communication systems, such as those used in 4G, require sophisticated VLSI architectures that minimize latency while maintaining robust signal integrity and high throughput.

Kim et al. [3] In their 2011 study, Kim and colleagues explored the VLSI design of a 16-QAM (Quadrature Amplitude Modulation) modulator based on CMOS technology, intended for use in wireless communication systems. CMOS technology is advantageous due to its low cost and high integration density, which allows for efficient implementation of complex systems on a single chip. The work demonstrated the feasibility of integrating high- order modulation schemes like 16-QAM into a single-chip solution, which is crucial for reducing the size and cost of wireless communication devices. The study emphasized the role of CMOS-based designs in developing cost-effective, high-performance systems for mid-to- high-speed wireless communications.

Zhang et al. [4] Zhang and collaborators (2012) focused on the design of high- speed modulator and demodulator systems using VLSI architecture. Their research specifically targeted the implementation of PSK (Phase Shift Keying) an d QAM (Quadrature Amplitude Modulation) systems in wireless communications. The study's contribution lies in the development of multi-stage processing for complex modulation schemes, ensuring that high data rates can be achieved without compromising signal quality. The key observation from their work was that, in high-speed communication systems, the balance between processing speed and power efficiency is critical. By using multi-stage VLSI designs, they were able to achieve both high data throughput and high performance without introducing significant power overhead.

Choi et al. [5] Choi and colleagues in their 2012 work concentrated on designing a low- power VLSI implementation of a 64-QAM modulator, which is typically used in high- data- rate communication systems. To minimize power consumption, they incorporated techniques such as clock gating and dynamic voltage scaling (DVS). for operation, which directly reduces power usage. The observation from their work was that even in high-order modulators, power consumption could be drastically

reduced through intelligent power management techniques, without sacrificing the modulator's performance. This made their design ideal for power-constrained systems, such as mobile devices and battery-operated communication equipment.

Sankar et al. [6] In 2013, Sankar et al. focused on low-power VLSI designs for BPSK (Binary Phase Shift Keying) modulators and demodulators, primarily targeting ultra- low- power communication systems. They explored techniques for reducing the total energy consumption of their modulator designs, which are crucial for systems where power efficiency is a top priority, such as IOT (Internet of Things) devices and other battery-operated wireless systems. Their work demonstrated that through the use of optimized circuit design and power management strategies, significant reductions in energy consumption could be achieved. The study highlighted the importance of creating power-efficient modulators that do not compromise performance, which is a key challenge in the design of modern wireless communication systems.

Nguyen et al. [7] Nguyen and his team (2014) presented their work on power- efficient VLSI designs for M-QAM (Multiple Quadrature Amplitude Modulation) modulators. These modulators, used in high-capacity wireless systems, are known for their complex signal processing requirements. Nguyen's research focused on minimizing both the area and power consumption of M-QAM modulators, which are critical for mobile communications. The authors used a combination of circuit-level optimizations, including the efficient use of multipliers and adders, to reduce the overall power footprint. Their observations reinforced the idea that power and area optimization should be a central focus when designing high- performance VLSI modulators, particularly in systems that demand high throughput and efficiency.

Kang et al. [8] Proposed a VLSI design for a MIMO system that integrates both modulator and demodulator functions, reducing complexity and improving communication efficiency. The study demonstrated that MIMO-based VLSI systems could achieve higher data throughput while maintaining low error rates.

U Penchalaiah, G. Suresh et al. [9] The proposed CNN-MAC accelerator addresses these challenges by integrating a Modified Booth Multiplier (MBM) and an Error Correctable Carry Look Ahead Adder (EC-CLA). The MBM enhances multiplication efficiency by reducing the number of partial products, while the EC-CLA minimizes propagation delay and corrects errors during addition, ensuring high-speed and reliable computation. This combination significantly improves the overall performance and energy efficiency of CNN accelerators, making them suitable for deployment in various high-demand scenarios.

3. PROPOSED SYSTEM

OTFS stands for Orthogonal Time Frequency Space. OTFS (Orthogonal Time Frequency Space) is a modern modulation scheme designed to enhance wireless communication, particularly in high-mobility environments, such as vehicular communications or satellite systems. It offers several advantages over traditional systems like OFDM (Orthogonal Frequency Division Multiplexing) in terms of robustness to Doppler shifts, delay spread, and interference, making it suitable for 5G and beyond. Orthogonal Time Frequency Space (OTFS) is a novel modulation technique that enhances traditional time-frequency approaches, such as OFDM, by introducing a two-dimensional time-frequency space (TFS) representation. In OTFS, the transmitted signal is mapped onto a dense and structured time-frequency grid, where each data symbol is spread across both time and frequency dimensions. This representation makes the system significantly more robust to Doppler shifts and delay spreads, which are common challenges in high-mobility environments. Unlike conventional systems that suffer performance degradation due to motion-induced frequency shifts, OTFS transforms the signal into a domain where Doppler effects manifest in a predictable manner, enabling more effective compensation at the receiver. Furthermore, OTFS incorporates space-time and space-frequency coding techniques to exploit spatial and frequency diversity, thereby improving reliability

and performance in dynamic wireless channels. Overall, OTFS offers superior resistance to interference, enhanced error resilience, and improved handling of fading and mobility compared to traditional modulation schemes.

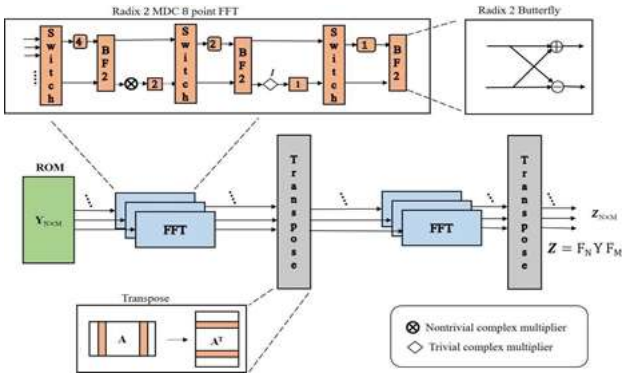


Fig. 1: Architecture details of the Z value computation from Y matrix.

This figure illustrates a hardware-efficient implementation of a Fast Fourier Transform (FFT)-based processing system using a Radix-2 Multi-Dimensional Cooley- Tukey (MDC) approach. The system is designed for efficient matrix transformations and is particularly useful in signal processing applications such as MIMO (Multiple-Input Multiple-Output) and OFDM (Orthogonal Frequency Division Multiplexing). The central part of the figure depicts a pipeline-based FFT processing system that operates on an input matrix YN×MY{N \times M}, stored in ROM. The FFT is applied to each column, followed by a transpose operation, another round of FFT processing, and a final transpose to obtain the transformed output ZN×MZ{N \times M}. This method follows the equation Z=FNYFMZ = F_N Y F_M, where FNF_N and FMF_M are the FFT transformation matrices along different dimensions.

4. RESULT AND DISCUSSION

Fig 2 shows the Proposed method results of the simulation for N=32, here A, B are consider the inputs and a simulation with inputs A and B, and outputs A' and B', the results for when N = 32when you input 1, it gives a certain output, and when you input 2, it gives same output, perfect match in the data.

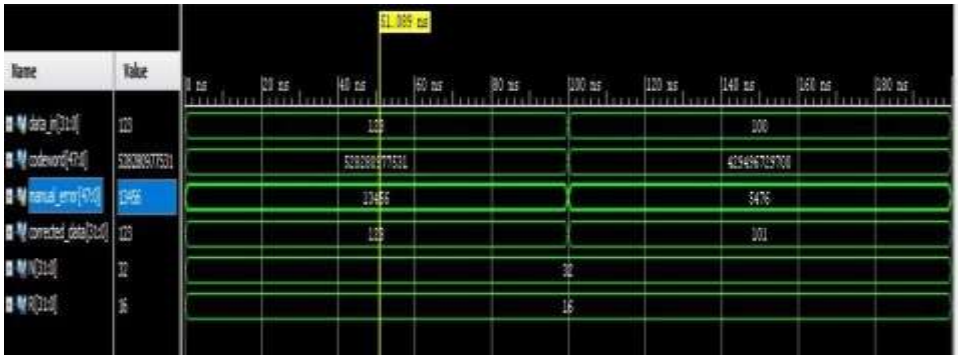
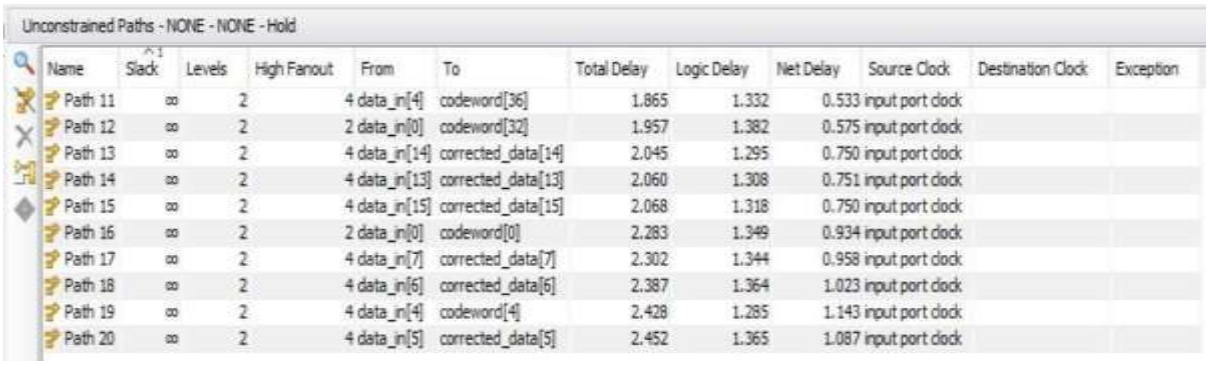


Fig. 2: Proposed Simulation Result for N=32

Fig. 3 shows Proposed power measurements for N=32. Here, the total power is 17.322 W, Static power includes PL Static power of 0.233 W, Dynamic power, signal power 17.089 W, Logic power of 0.014 W, and I/O power of 16.040 W.

Fig. 3: Proposed power for N=32.


Unconstrained Paths - NONE - NONE - Hold

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Source Clock	Destination Clock	Exception
Path 11	∞	2	4	data_in[4]	codeword[36]	1.865	1.332	0.533	input port clock		
Path 12	∞	2	2	data_in[0]	codeword[32]	1.957	1.382	0.575	input port clock		
Path 13	∞	2	4	data_in[14]	corrected_data[14]	2.045	1.295	0.750	input port clock		
Path 14	∞	2	4	data_in[13]	corrected_data[13]	2.060	1.308	0.751	input port clock		
Path 15	∞	2	4	data_in[15]	corrected_data[15]	2.068	1.318	0.750	input port clock		
Path 16	∞	2	2	data_in[0]	codeword[0]	2.283	1.349	0.934	input port clock		
Path 17	∞	2	4	data_in[7]	corrected_data[7]	2.302	1.344	0.958	input port clock		
Path 18	∞	2	4	data_in[6]	corrected_data[6]	2.387	1.364	1.023	input port clock		
Path 19	∞	2	4	data_in[4]	codeword[4]	2.428	1.285	1.143	input port clock		
Path 20	∞	2	4	data_in[5]	corrected_data[5]	2.452	1.365	1.087	input port clock		

Fig. 4: Proposed Setup Delay for N=32

Fig 4 shows Proposed Setup delay for N=32. Here, maximum Total Delay is 12.602 ns, maximum Logic Delay is 3.314 ns, maximum Net Delay is 9.346 ns**.**

5. CONCLUSION

The OTFS (Orthogonal Time Frequency Space) project has explored a ground breaking approach to wireless communication, focusing on enhancing performance in challenging environments, particularly in high-mobility scenarios. Traditional communication methods, like Orthogonal Frequency Division Multiplexing (OFDM), face difficulties in dealing with severe Doppler shifts and rapidly changing channel conditions. OTFS, however, addresses these issues by mapping the transmitted signal in the time-frequency space, which allows for better resilience against interference and distortions caused by mobility. By utilizing a two- dimensional signal representation, OTFS shows promise in significantly improving signal reliability and capacity in real-world, high-speed applications. Throughout the project, OTFS's potential advantages over conventional methods were showcased, particularly its ability to improve spectral efficiency and reduce the impact of interference. The technique allows for better channel utilization and more robust transmission, even in scenarios with high Doppler effects or poor channel conditions, such as urban or satellite communication environments. The project demonstrated that OTFS could outperform OFDM in terms of both error performance and throughput, particularly in dynamic environments where traditional

techniques struggle.In conclusion, the OTFS project has established the technique as a powerful candidate for next- generation wireless communication systems, including 5G and beyond. Its ability to handle mobility-induced channel impairments effectively opens new opportunities for high-performance networks, especially in critical areas like autonomous driving, mobile broadband, and satellite communication. The findings suggest that OTFS could play a key role in the development of more reliable, efficient, and high-capacity communication systems, paving the way for more robust and scalable networks in the future.

REFERENCES

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for operation, which directly reduces power usage. The observation from their work was that even in high-order modulators, power consumption could be drastically reduced through intelligent power management techniques, without sacrificing the modulator's performance. This made their design ideal for power-constrained systems, such as mobile devices and battery-operated communication equipment.

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[9] **U. Penchalaiah, G. Suresh, K. S. Kumar, G. Tejaswi and A. H. Krishna,** "Scalable CNN Accelarator with Error-Correcting Accumulator for High-Performance Deep Learning Applications," 2024 International Conference on Distributed Systems, Computer Networks and Cybersecurity (ICDSCNC), Bengaluru, India, 2024, pp. 1-6, doi: 10.1109/ICDSCNC62492.2024.10939145.